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D E C P D P - 1 1

E N G I N E E R S G U I D E

Assembled By J. Dunkley T.S.C.

Issue 3: 18.11.83

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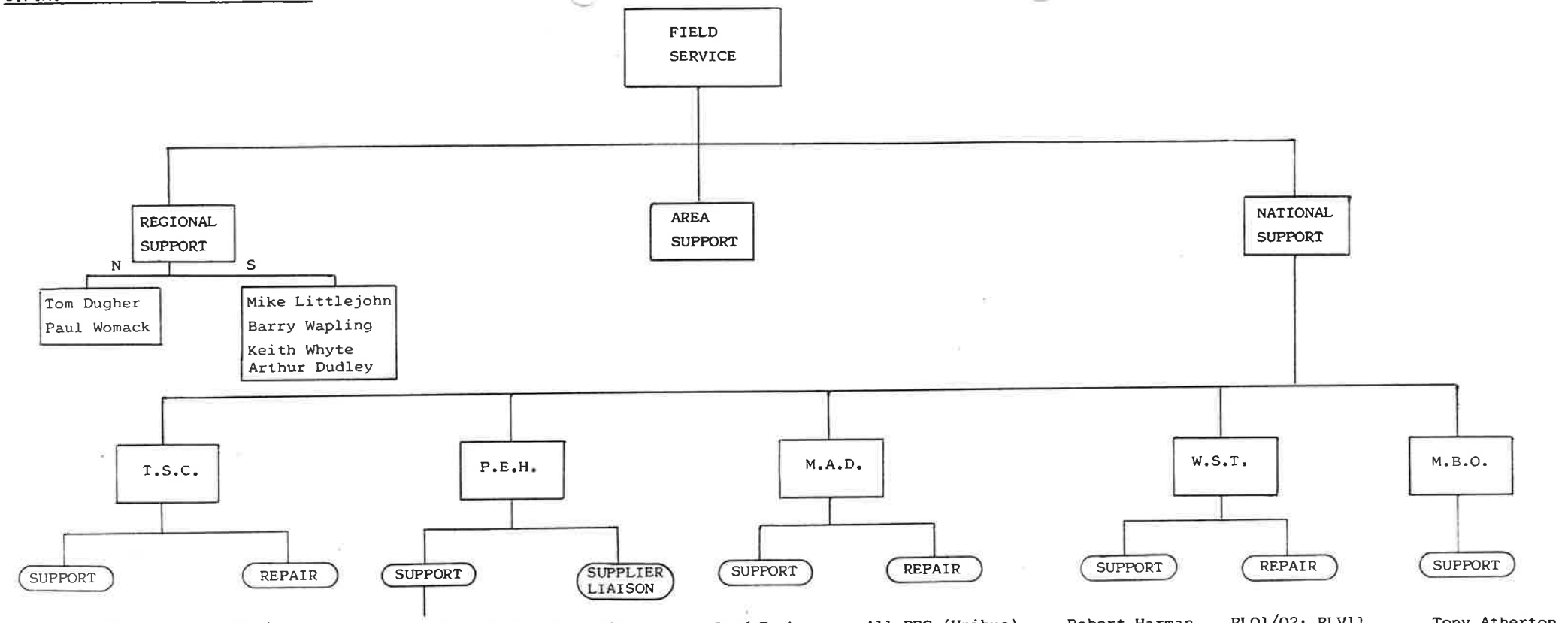

Dave Hutton

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Jim Dunkley

1134: 1124: RL01/02
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Dave Hazelwood

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T.S.11
Digi Data
1123 C.P.U.
B300/600

Simon Koumparous : VAX

Derek Simpson : LSI: WILKES
GR: ARROW
HOSKYNS

Bill Hanmore : DEC UNIBUS
DATALOGIC
SYSTEM
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Steve Sullivan: COMMISSIONING
INSTALLATION

Geof Parker

Mike Blackshaw

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1105 CPU

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Systime
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} addon's

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Robert Harman

Tony Dargis

Mike Dumville

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SMD/CMD
Controllers

Tony Atherton

Trudi Holt

Nic Bliss

UNIBUS

The UNIBUS is an outstanding design feature that makes possible the strengths and flexibilities of the PDP-11 family members discussed in this book. DIGITAL's unique data bus, the UNIBUS, provides the hardware and software backbone of the PDP-11/04, PDP-11/24, PDP-11/34A, PDP-11/44 and PDP-11/70 processors. The UNIBUS was the first data bus in the history of the minicomputer industry to enable devices to send, receive, or exchange data without processor intervention and without intermediate buffering in memory.

PDP-11 ARCHITECTURE AND THE UNIBUS

PDP-11 architecture takes advantage of the UNIBUS in its method of addressing peripheral devices. Memory elements, such as the main core memory, or any read-only or solid state memories, have ascending addresses starting at zero, while registers that store I/O data or the status of individual peripheral devices have addresses in the highest 8K bytes of addressing space.

There are tens of thousands of memory addresses, but only two—one for data, one for control—for some peripheral devices, and up to half a dozen for more complicated equipment like magnetic tapes or disks.

The PDP-11 UNIBUS consists of 56 signal lines, to which all devices, including the processor, are connected in parallel.

51 lines are bidirectional and 5 are unidirectional.

Communication between any two devices on the bus is in a master/slave relationship. During any bus operation, one device, the bus master, controls the bus when communicating with another device on the bus, called the slave. For example, the processor, as master, can fetch an instruction from the memory, which is always a slave; or the disk, as master, can transfer data to the memory, as slave. Master/slave relationships are dynamic: the processor, for example, may pass bus control to a disk, then the disk may become master and communicate with slave memory.

When two or more devices try to obtain control of the bus simultaneously, priority circuits decide between them. Devices have unique priority levels, fixed at system installation. A unit with a high priority level obviously always takes precedence over one with a low priority level; in the case of units with equal priority levels, the one electrically closest to the processor on the bus takes precedence over those further away.

Suppose the processor has control of the bus when three devices, all of higher priority than the processor, request bus control. If the requesting devices are of different priority, the processor will grant use of the bus to the one with the highest priority. If they are all of the same priority, all three signals come to the processor along the same bus line, so that it sees only one request signal. Its reply granting priority travels down the bus to the nearest requesting device, passing through any intervening nonrequesting devices. The requesting device takes control of the bus, executes a single bus cycle of a few hundred nanoseconds, and relinquishes the bus. (Some devices will take the bus for more than one bus cycle.) Then the request grant sequence occurs again, this time going to the second device down the line, which has been waiting its turn. When all higher-priority requests has been granted, control of the bus returns to the lowest-priority device, usually the processor.

The processor usually has lowest priority because in general it can stop whatever it is doing without creating serious consequences. Peripheral devices may be involved with some kind of mechanical motion, or may be connected to a real-time process, either of which requires immediate attention to a request, to avoid data loss.

The priority arbitration takes place asynchronously in parallel with data transfer. Every device on the bus except memory is capable of becoming a bus master.

BUS COMMUNICATION

Communication is interlocked, so that each control signal issued by the master must be acknowledged by a response from the slave to complete the transfer. This simplifies the device interface because timing is no longer critical. The maximum transfer rate on the UNIBUS is one 16-bit word every 400 ns, or about 2.5 million 16-bit words per second. However, the typical transfer rate including average bus delays, is 1 million 16-bit words per second.

USING THE BUS

A device uses the bus if it needs to:

- Request the processor. As a result, the processor stops what it is doing, enters an interrupt service routine, and services the device.
- Transfer a word or byte of data to or from another device, (usually memory), without involving the processor, an NPR (nonprocessor request) transfer. Such functions are performed by direct memory access devices such as disks or tape units.

Whenever two devices communicate, it is called a bus cycle. Only one word or byte can be transferred per bus cycle. An instruction cycle

involves one or more bus cycles. Fetching an instruction involves a bus cycle; storing a result in memory or a device register involves another bus cycle.

BUS CONTROL

There are two ways of requesting bus control: nonprocessor requests (NPRs) or bus requests (BRs).

An NPR is issued when a device wishes to perform a data transaction. An NPR device does not use the CPU once the running program has set up parameters of buffer address, disk sector selection and byte count; therefore, the CPU can relinquish bus control while an instruction is being executed.

A BR is issued when a device needs to interrupt the CPU for service. An interrupt is not serviced until the processor has finished executing its current instruction.

Bus Requests

- DEVICE makes a bus request by asserting a BR.
- BUS ARBITRATOR recognizes the request by issuing a Bus Grant (BG). This bus grant is issued only if the priority of the device is greater than the priority currently assigned to the processor.
- DEVICE acknowledges the bus grant and inhibits further grants by asserting Selection Acknowledge (SACK). The device also clears BR.
- BUS ARBITRATOR receives SACK and clears BG.
- DEVICE asserts Bus Busy (BBSY) and clears SACK.
- DEVICE asserts Bus Interrupt (INTR) and its vector address.
- CPU responds

Nonprocessor Requests

- DEVICE makes a nonprocessor request by asserting NPR.
- BUS ARBITRATOR recognizes the request by issuing a nonprocessor grant or NPG.
- DEVICE acknowledges the grant and inhibits further grants by asserting SACK; device also clears NPR.
- BUS ARBITRATOR receives SACK and clears NPG.
- DEVICE asserts Bus Busy (BBSY) and clears SACK.
- DEVICE starts its data transfer.

BUS BUSY SIGNAL

Once a device's bus request has been honored, it becomes bus master after the current bus master relinquishes control.

- Current bus master relinquishes bus control by clearing bus busy (BBSY).
- New device assumes bus control by setting BBSY.

INTERRUPTS

Interrupt handling is automatic in the PDP-11. No device polling is required to determine which service routine to execute. A device can interrupt the CPU only if it has gained bus control via a BR. The DEVICE requests an interrupt by asserting INTR along with an interrupt vector. The vector directs the CPU to a memory location previously loaded by the running program with the starting address of an interrupt service routine (ISR). ("I need to interrupt.") The CPU accepts the interrupt vector an asserts SSYN (Slave SYNC) to indicate the vector has been accepted. ("I have your interrupt.") The DEVICE releases the bus to the CPU by clearing INTR, removing the vector, and clearing BBSY. ("I'm giving control of the bus back to you.") The CPU acknowledges by clearing SSYN (Slave SYNC), stores the information it needs to return to the interrupted program (a hardware stack located in memory is used for this purpose), and enters the interrupt handling sequence. ("Thank you, I'm starting to service your interrupt.") When the interrupt operation is completed, the CPU removes the information that was stored on the stack and resumes the program at the point where it was interrupted. A more detailed description of the operations required to service an interrupt follows:

1. Processor relinquishes control of the bus, priorities permitting.
2. When a master gains control, it sends the processor an interrupt request and a unique memory address which contains the address of the device's service routine, called the interrupt vector address. Immediately following this pointer address is a word (located at vector address + 2) which is to be used as the new processor status (PS) word.
3. The new PC and PS (interrupt vector) are taken from the specified address. The old PS and PC are pushed onto the current stack. The service routine is then entered when the contents of the vector address are moved to the PC and program execution resumes—at the address of the interrupt service routine (ISR) loaded previously as a vector by the running program
4. The device service routine can cause the processor to resume the interrupted process by executing the Return from Interrupt instruction, described in Chapter 4, which pops the two top words from the current processor stack and uses them to load the PC and PS registers.

A device routine can be interrupted by a higher priority bus request any time after the new PC and PS have been loaded. If such an interrupt occurs, the PC and PS of the service routine are automatically stored in the temporary registers and then pushed onto the new current stack, and the new device routine is entered. This is known as "nesting."

Interrupt Servicing

Every hardware device capable of interrupting the processor has a unique pair of locations (two words) reserved for its interrupt vector in low memory. The first word contains the location of the device's service routine, and the second, the processor status word that is to be used by the service routine. The program is responsible for loading the address of the ISR into this low memory address before interrupt time occurs. Through proper use of the PS, the programmer can switch the operational mode of the processor, and modify the processor's priority level to mask out lower level interrupts.

PRIORITY CONTROL

The PDP-11 priority system determines which device obtains the bus. Each PDP-11 device is assigned a specific location in the priority structure. Priority arbitration logic determines which device obtains the bus according to its position in the priority structure. The priority structure is 2-dimensional; i.e., there are vertical priority levels and horizontal priorities at each level. There are five vertical priority levels.

Devices that gain bus control with one of the bus request lines (BR7, BR6, BR5, BR4) can take full advantage of the power of the processor by requesting an interrupt. The entire instruction set is then available for manipulating data and status registers. When a device servicing program is being run, the task being performed by the processor is interrupted, and the device service routine is initiated. After the device request has been satisfied, the processor returns to its former task. Note that interrupt requests can be made only if bus control has been gained through a BR priority level.

Bus Request Level

There are two lines associated with each BR level. The bus request is made on a BR line (BR7, BR6, BR5, or BR4). The bus grant is made on the corresponding grant line (BG7, BG6, BG5, or BG4). BR levels BR3 through BR0 are used only by the software; devices are not assigned to these BR levels. Unlike NPRs, a BR can be handled only between instruction cycles. The BR levels are used for interrupts so that the device can obtain service from the CPU. A request made at any BR level requires processor intervention.

Priority Levels

Because there are only five vertical priority levels, NPR, BR7, BR6, BR5 and BR4, it is often necessary to connect more than one device to a single level. When a number of devices are connected to the same level, the situation is referred to a horizontal priority. If more than one device makes a request at the same level, then the device electrically closest to the CPU has the highest priority.

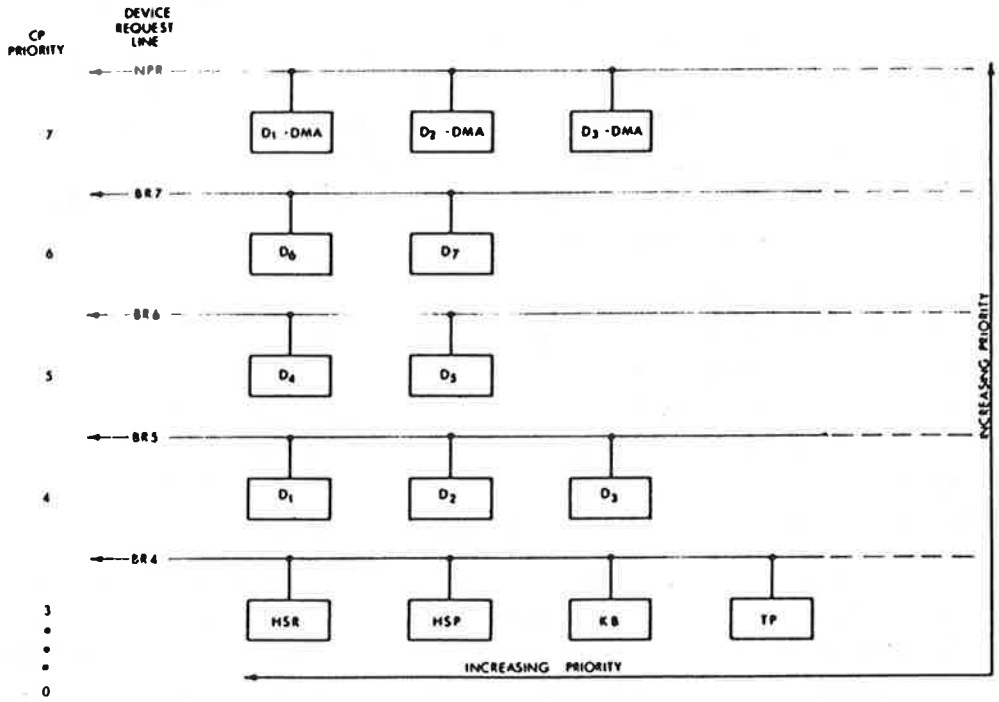


Figure 2-2 Priority Control

The grant line for the NPR level is connected to all devices on that level in a "daisy chain" arrangement. When an NPG is issued, it first goes to the device electrically closest to the CPU. If that device did not make the request, it permits the NPG to travel to the next device. Whenever the NPG reaches a device that has made a request, that device captures the grant, and prevents it from passing to any subsequent device in the chain.

BR chaining is identical to NPR chaining in function. However, each BR level has its own BG chain. Thus, the grant chain for BR7 is the BG7 line which is chained through all devices at the BR7 level.

PRIORITY ASSIGNMENTS

When assigning priorities to a device, three factors must be considered: operating speed, ease of data recovery, and service requirements.

Data from a fast device may be available for only a short time period. Therefore, highest priorities are usually assigned to fast devices to prevent loss of data and to prevent the bus from being tied up by slower devices.

If data from a device are lost, recovery may be automatic, may require manual intervention, or may not be possible. Therefore, highest priorities are assigned to devices whose data cannot be recovered, while lowest priorities are reserved for devices with automatic data recovery features.

CPU Priority Level

In addition to device priority levels, the CPU has a programmable priority. The CPU can be set to any one of eight priority levels. Priority is not fixed; it can be raised or lowered by software. The CPU priority is elevated from level 4 to level 6 when the CPU stops servicing a BR4 device and starts servicing a BR6 device. This programmable priority feature (the second vector word) permits masking of bus requests. The CPU can hold off servicing lower priority devices until more critical functions are completed. For example, when CPU priority is set to level 6, all bus requests on the same and lower levels are ignored (in this case, all requests appearing on BR4, BR5, and BR6).

DATA TRANSACTIONS

There are four types of data transactions:

- DATO—a data *word* is transferred out of the master and into its slave.
- DATOB—a data *byte* is transferred out of the master and into its slave.
- DATI—a data word is transferred from the slave to the master. The master may select the low or high byte if only a data byte is desired.
- DATIP—used with destructive readout devices such as core memory. It is similar to a DATI except that data are not rewritten (restored) into the addressed memory location (data are restored during a DATI) unless followed by DATO or DATOB to the same location.

EXECUTION OF DATA TRANSACTIONS

Before a device can perform a data transaction, it must:

- Obtain control of the bus via an NPR.

- Select (address) the slave device it wishes to communicate with. Each device on the bus has a unique address.
- Tell the slave what type of data transaction is to be performed.
- Wait for a response from the slave indicating the slave is present and ready.

Data transactions between a master and a slave device are synchronized by master sync (MSYNC) and slave sync (SSYN) signals. Below is an example of how these signals are used during a typical DATI transaction:

1. Master selects the slave by addressing it, specifies the type of data transaction, and requests data by asserting MSYN. ("Give me data.")
2. Slave gathers the data and asserts SSYN when the data are available. ("Here it is.")
3. Master drops MSYN after it accepts the data. ("Thank you, I have the data.")
4. Slave removes data from the lines and acknowledges the master by dropping SSYN. ("You're welcome.")

Table 2-1 Bus Control

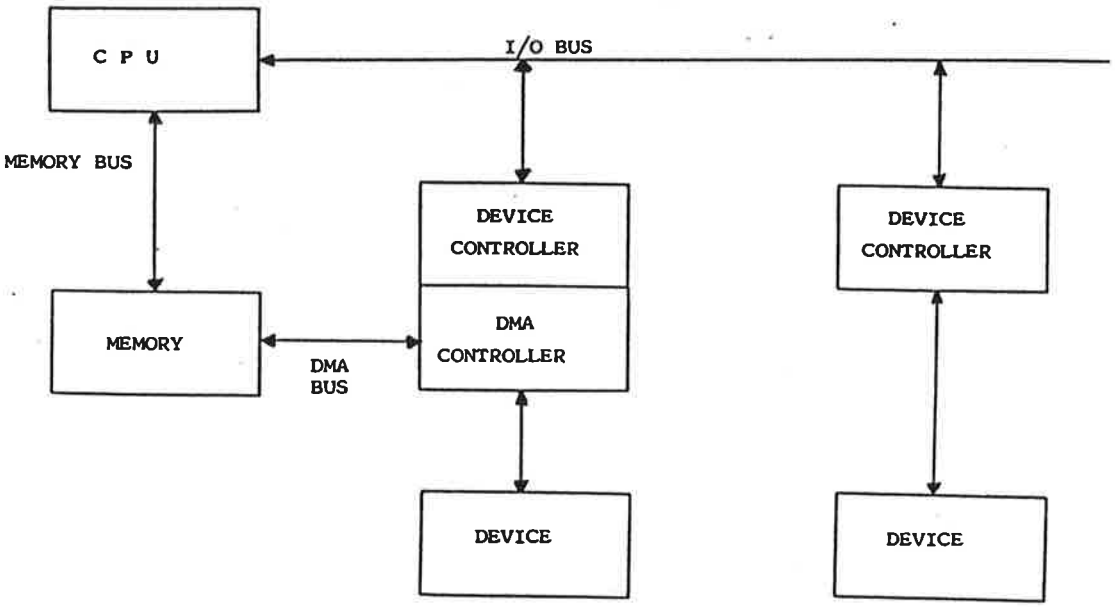
Signal	Name	Source	Dest.	Timing	Function
NPR	Non-processor Request	Any DMA device	UNIBUS Control LOGIC	Asynchronous	Highest priority bus request
NPG	Non-processor Grant	CPU	Next bus master	Asynchronous	Transfers bus control
BR7 through BR4	Bus Request	Any device	UNIBUS Control LOGIC	Asynchronous	Requests bus control
BG7 through BG4	Bus Grant	Memory	Next bus master	After instruction	Transfers bus control
SACK	Selection Acknowledge	Next bus master	UNIBUS Control LOGIC	Response to NPG or BG	Acknowledges grant and inhibits further grants
BBSY	Bus Busy	Master	All devices	Asserted by bus master	Asserts control of the bus
INTR	Interrupt	Master	UNIBUS Control LOGIC	If control has been gained by a BR (not NPR), INTR asserted after BBSY	Transfers bus control to handling routine in the processor

PDP-11 vs TRADITIONAL SYSTEM

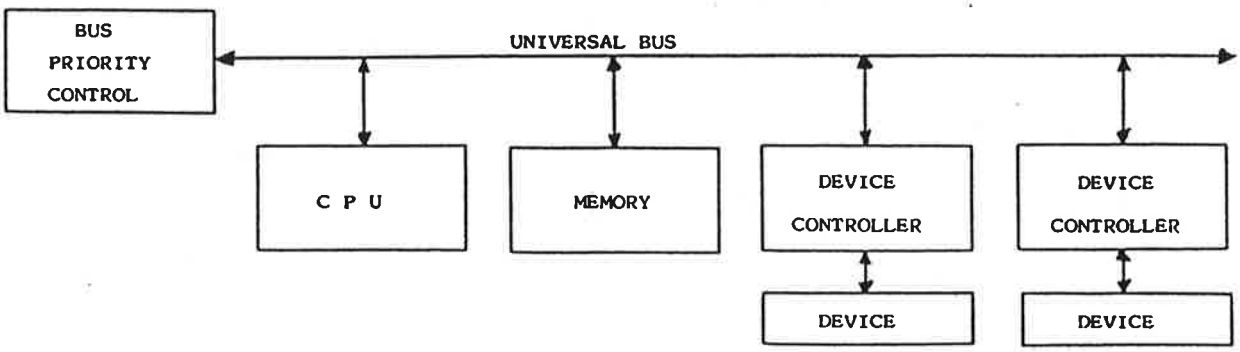
The two primary differences between PDP-11 and Traditional Computers are:

1 The system of interconnection.

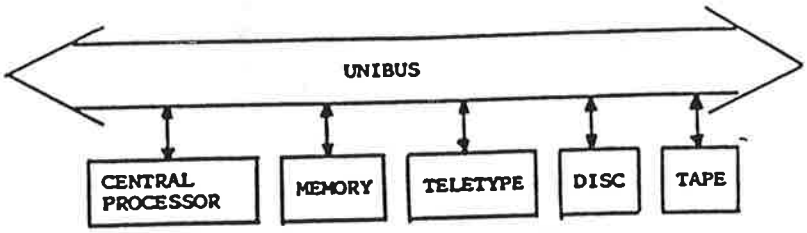
2 The instruction set.



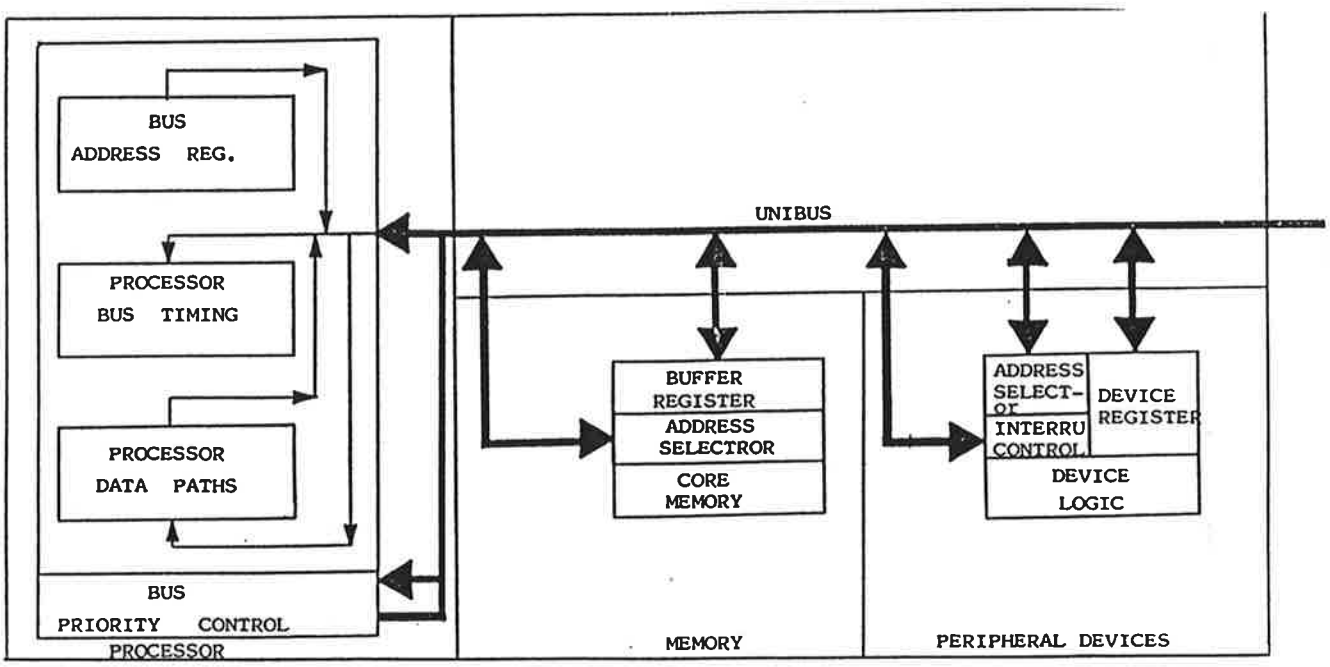
CONVENTIONAL I/O BUS



UNIVERSAL BUS



- Bidirectional
- Asynchronous, interlocked
- Dynamic ownership
- I/O addressable as memory
- Data signals, ownership signals
- Vectored interrupt
- Standard specifications



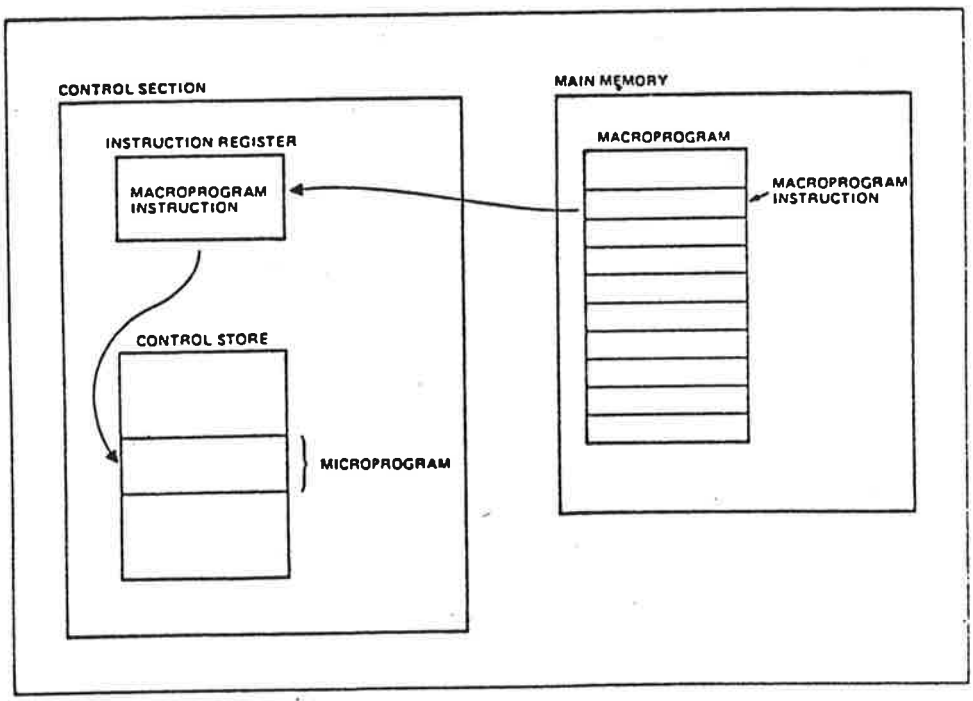
UNIBUS

T7 3.19

Microprogramming

- Control store instead of fixed wired hardware
- Macro instruction (normal instruction) = microprogram
- User can tailor minicomputer instruction set
- Speed
- Emulation

T7 3.20



Microprogram

CAPABILITIES PROVIDED BY MEMORY MANAGEMENT

Memory Size (words):	124K, max (plus 4K for I/O & registers).
Address Space:	Virtual (16-bits).
	Physical (18-bits).
Modes of Operation:	Kernel & User.
Stack Pointers:	2(One for each mode).
Memory Relocation: Number of Pages:	16(8 for each mode).
Page Length:	32 to 4,096 words.
Memory Protection:	No access.
	Read only.
	Read/Write.

When in Kernel mode, the program has complete control and can execute all instructions. Monitors and supervisory programs are executed in this mode.

When in User mode, the program is prevented from executing certain instructions that could:-

- Cause the modification of the Kernel program.
- Halt the computer.
- Use memory space assigned to the kernel or to other users.

In a multi-programming environment several user programs would be resident in memory at any given time. The task of the supervisory program would be to:-

- Control the execution of the various user programs.
- Allocate memory and peripheral device resources.
- Safeguard the integrity of the system as a whole by careful control of each user program.

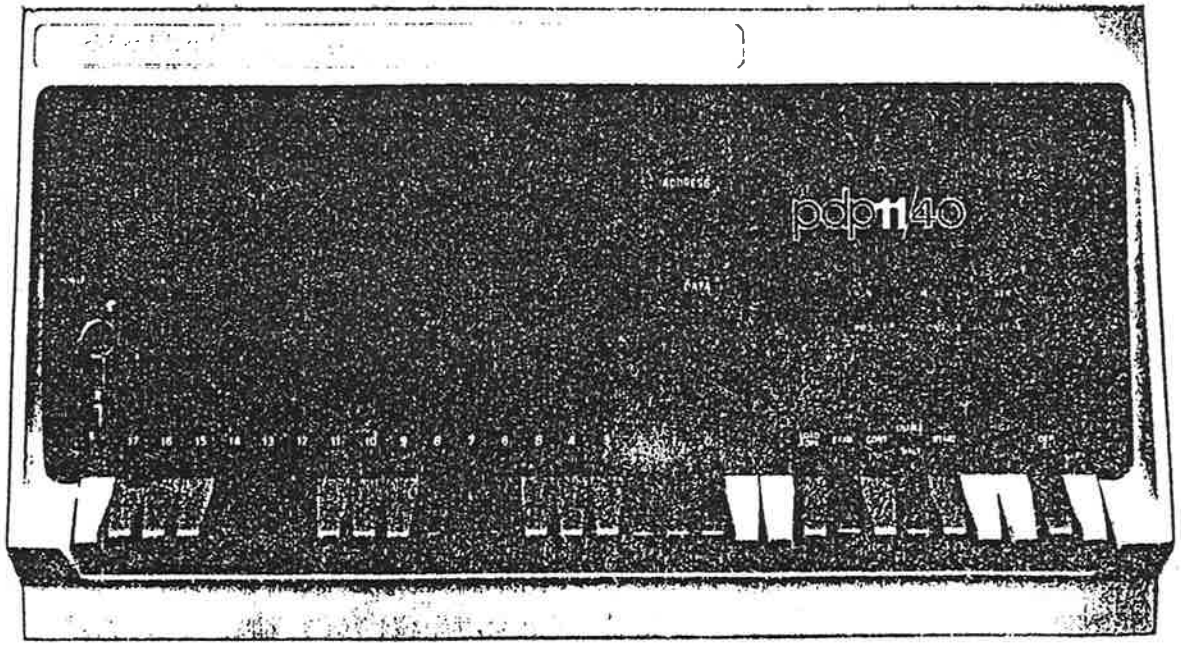
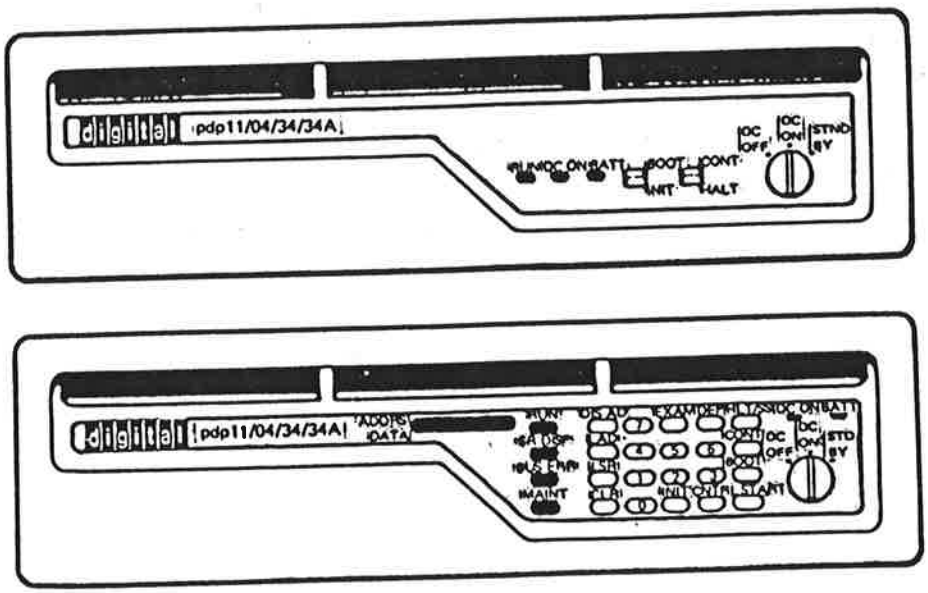


Figure 3-1a PDP-11/40 Programmer's Console

Traditionally, the PDP-11 family of computers has utilized a front panel which contained a switch register and light display that allowed the user to communicate with the machine.

The 11/04/34 computers introduce the next generation of DEC Man-machine interfaces which communicate with the user via the system terminal, This new generation of machine is symbolized by the simple, distinctive Operator's Console and the graphical record of the Operator-Machine dialogue.



DEC Modules and processor types can present a confusing array of mnemonic, module number and description. There is a vague logic behind DEC's philosophy which in order to understand fully, require us to define certain elements of a module.

Each module can be described under three seperate headings.

1) Mnemonic (DL11)

2) Module Number (M7800)

3) Description (Asynchronous Line Unit)

Mnemonics are used to describe a family of devices, (i.e. Disc Drives) and specific types within that family.

Family:-

c)	Processors		K
b)	Memory Management	(Suffix)	KT
c)	Cach Memory	(Suffix)	KK
d)	Floating Point Processors		F
e)	Memory		M
f)	Serial Line Units		D ← communication devices.
g)	Line Printer Interfaces		L
h)	Disc Drives/Controllers		R
j)	Tape Drives/Controller		T

Device Mnemonics are presented in the form A.B.11 or (XX).

Where A = Device Family (i.e. Discs) R
B = Device Type (i.e. RK) K
11 = System Type (PDP11)
XX = Generic number of device (i.e. 05)

So that the RK11 would be the unibus controller for a number of RK05 Disc Drives.

Beware of mnemonics to boot these devices (RK05 = DK)

Modules : are presented in the form:

X 1 2 3 4

Alpha Numeric

Where the alpha character relates to:-

A Analogue Devices

B Descreet Logic

G Analogue Sense Amps (Memory and Tape)

H P.S.U's, Core Stack's, Test Connectors and Cabinets

M Intigrated Logic Module

The numeric is a generic module reference, with no logical approach regarding devices.*

* With one exception, M900/9000 series of modules are applicable to unibus devices i.e. terminators, jumpers, and bootstraps etc.

DEVICE MNEMONICS

AA	AA11, AAV11	IR	ICR-11	PA	PA611, TYP-11
AD	AD11, ADV11, ADO1	IT	ITEP	PC	PC11, PCS11
AF	AFC11	KA	CPU	PL	PCL11
AR	AR11	KB	CPU	PM	PDM-70
BB	KIT-11	KC	CPU	QE	CPU
BM	BM873, BDV-11	KD	CPU	QM	MEMORY
BT	BUS TESTER	KE	CPU	QK	CPU
CB	CB11	KG	CPU	QU	DEC/X11
)	CD11	KH	KIT-11	R6	RK611, RKO6/7
L	CL11	KL	KL11	RC	RC11
M	CM11	KK	CACHE MEMORY	RF	RF11
CP	CPU	KM	KMC11, MEMORY	RH	RH70
CT	CT11	KT	MEMORY MANAGEMENT	RJ	RP04/5/6
CR	CR11	KU		RK	RK11, RKO5
DC	DC11	KW	KW11, KWV11	RL	RL11, RLV11, RLO1/2
DF	DFC11	LA	LA11, LC11, DEC PRINTERS	RM	RH11, RH70, RMO2/3
DH	DH11	LC	LC11	RP	RP11, RPO2/3
DJ	DJ11	LK	LK11	RS	RH11, RSO3/4
DL	DL11, DLV11	LP	LP11, LPx-11	RT	RTO1/2
DM	DM11, DMx11	LQ	LQP	RX	RX11, RX21, RXV11, RXO1
DN	DN11	LS	LS11	TA	TA11
	DP11, DUP11	LV	LV11	TC	TC11
)	DQ11	M9	M9301, M9312	TE	TE16, TU77, TM03
DR	DR11, DRV11	MF	MEMORY	TM	TM11, TMA11, TE10
DT	DTO7, DTE20	MJ	MEMORY	TR	TR79F
DU	DU11, DUV11	MK	MEMORY	TS	TS11
DV	DV11	ML	MEMORY	TU	TMO2, TU10
DX	DX11	MM	MEMORY	UD	UDC11
DZ	DZ11, DZV11	MN	MNC-11	VS	VS60
FP	FP11	MR	MR11	VT	VT
GT	GT40, GT44	MS	MEMORY	XY	XY11
IB	IBV-11	NC	NC11, NCV11		

BACKPLANES

BB11 = Blank

DD11A = 4 spc

DD11B = 4 spc + 2 DF11 (instead of power card)

DD11C 4 slot [redacted] expander

DD11D 9 slot [redacted] expander

DD11E ?

DD11DK mod unibus 9 slots

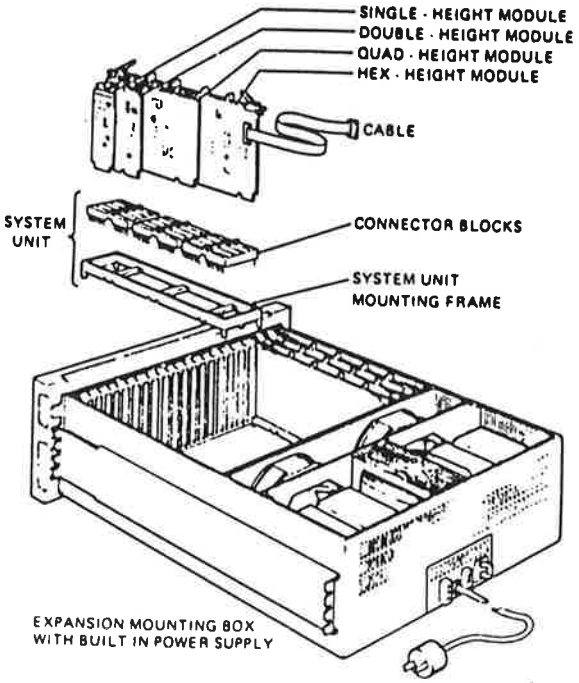
DD11-PK 9 slot modified with processor (slot 1)

DD11-CK 4 slot modified with processor

NOTE:

DD11 PK OK in BA11L & BA11K only

DD11 PF Only in BA11F & BA11P



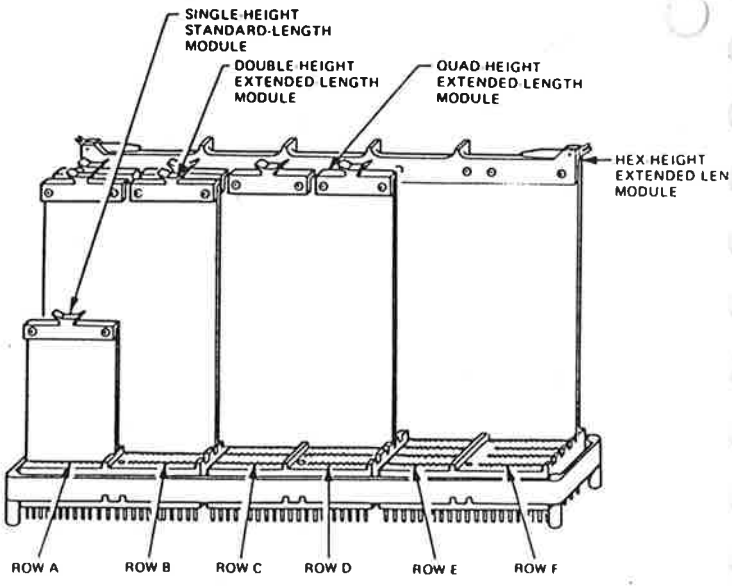
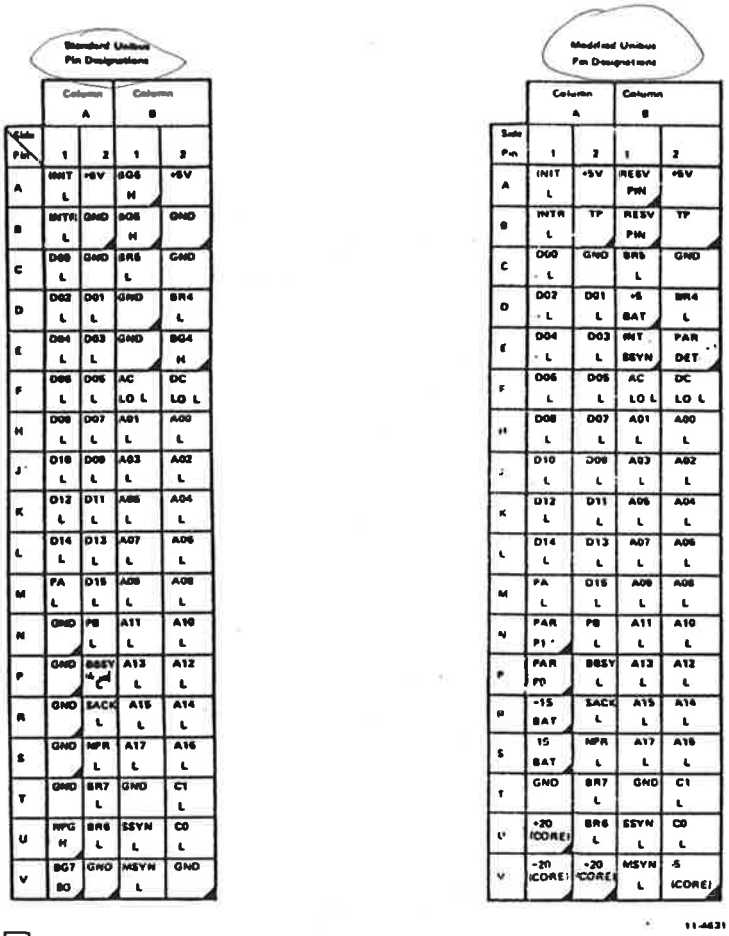


Figure 2 Typical Subsystem



NOTE: ◪ Indicates a redesignated pin.

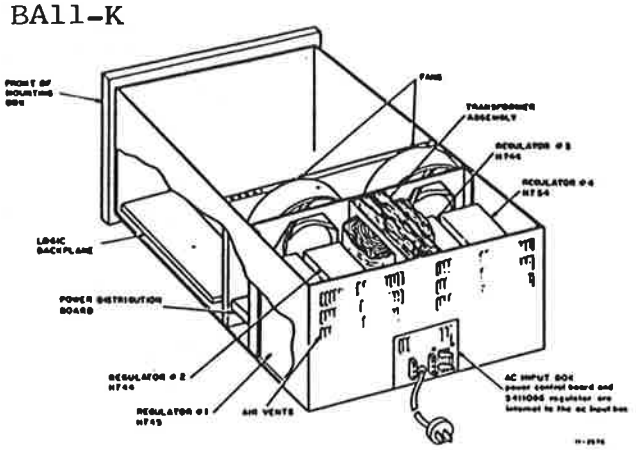
Side / Pin	Column C 1	Column C 2	Column D 1	Column D 2	Column E 1	Column E 2	Column F 1	Column F 2
A	NPG (IN)	+5V	TP	+5V	GND A	+5V	ABG OUT	+5V
B	NPG (OUT)	-15V	TP	-15V	ASSYN IN H	-15V	ABG IN	-15V
C	PA L	GND	A SEL 5	GND	A12 L	GND	SSYN L	GND
D	LTC	D15 L	A OUT LOW	BR7 L	A17 L	A15 L	BBSY L	FO1 N1
E	TP	D14 L	A SEL 4	BR6 L	MSYN L	A16 L	FO1 V2	D02 L
F	TP	D13 L	A SEL 0	BR5 L	A02 L	C1 L	D05 L	D06 L
H	D11 L	D12 L	A IN	BR4 L	A01 L	A00 L	D07 L	A INT ENB B
J	A INT B	D10 L	A SEL 2	A BR OUT	SSYN L	C0 L	NPR L	GND A
K	TP	D09 L	A OUT	BG7 SO	A14 L	A13 L	D06 L	A INT B
L	A INT ENBB	D08 L	INIT L	BG7 OUT	A11 L	TP	D03 L	FO1 L2
M	TP	D07 L	AINT ENBA	BG6 SO	AIN	AOUT HIGH	INTR L	FO1 M2
N	DC LO	D04 L	A INT A	BG6 OUT	A OUT LOW	A08 L	FO1 N1	D04 L
P	HALT REQ	D05 L	TP	BG5 SO	A10 L	A07 L	ABR OUT	FO1 P2
R	HALT GRT	D01 L	TP	BG5 OUT	A09 L	ASEL 4	FO1 L2	FO1 N1
S	PE L	D00 L	TP	BG4 SO	ASEL 6	ASEL 0	FO1 M2	FO1 P2
T	GND	D03 L	GND	BG4 OUT	GND	ASEL 2	GND	SACK L
U	-15/-8	D02 L	TP	ABG IN	A06 L	A04 L	A INT A	ABR OUT
V	AC LO	D06 L	ASSYN IN H	ABG OUT	A05 L	A03 L	A INT ENB A	FO1 FO1

11-4630

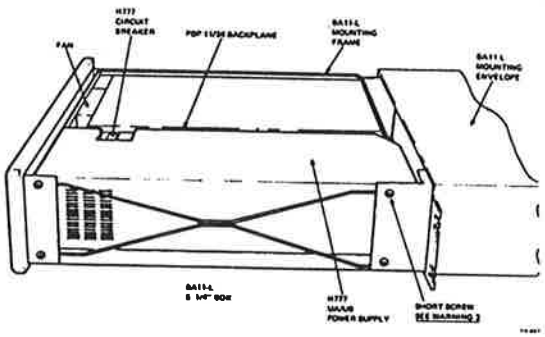
Figure 4-5 SPC Pin Designations

MOUNTING BOXES

BA11-K

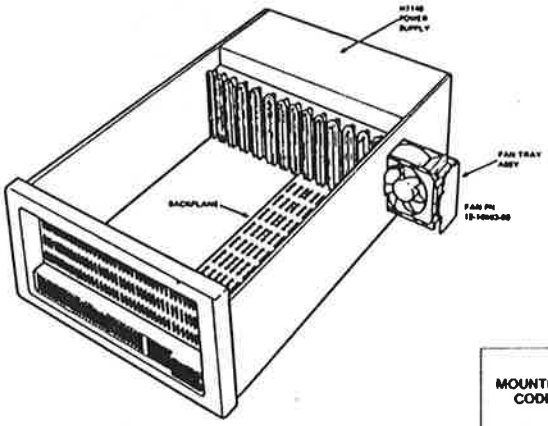


BA11-L



BA11-L 5 1/4 Inch Box

BA11-A



EXPANSION BOXES

	BA11-KE (KF)	BA11-KW (KX)	BA11-LE (LF)
MOUNTING CODE	10.5 in (26.7 cm) PANEL SPACE	10.5 in (26.7 cm) PANEL SPACE	5.25 in (13.3 cm) PANEL SPACE
MOUNTING SPACE PROVIDED	5 SYSTEM UNITS	5 SYSTEM UNITS	2 SYSTEM UNITS
CURRENT DRAWN	12 A ~ 120 Vac	12 A ~ 120 Vac	5 A ~ 120 Vac
CURRENT AVAILABLE	50 A ⎓ + 5 Vdc 4 A ⎓ + 15 Vdc 10 A ⎓ - 15 Vdc	50 A ⎓ + 5 Vdc 4 A ⎓ + 15 Vdc 10 A ⎓ - 15 Vdc	32 A ⎓ + 5 Vdc 2 A ⎓ + 15 Vdc 2 A ⎓ - 15 Vdc
REQUIRED CABINETRY SYSTEMS	H960 SERIES	H9640 SERIES H9600 SERIES	PDP-11/24, PDP-11/34A & PDP-11/44 SYSTEMS
CABLE INCLUDED	BC11A	BC11A	BC11A

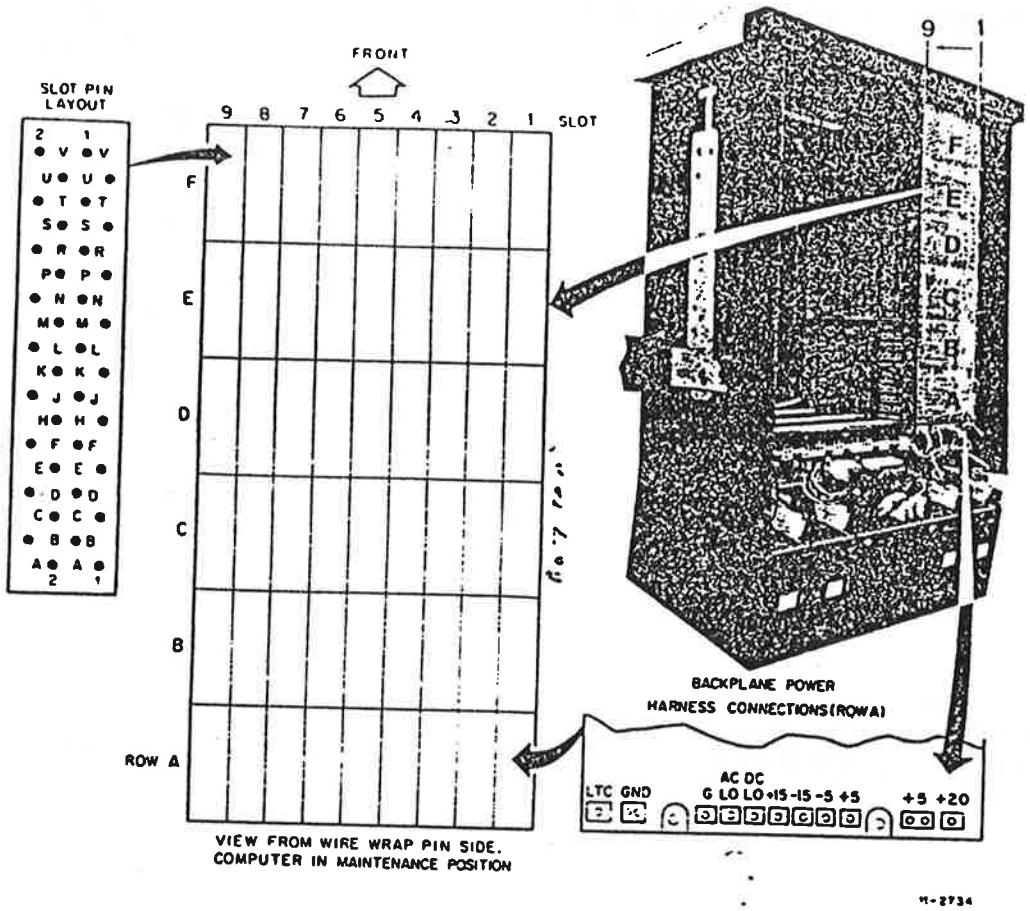
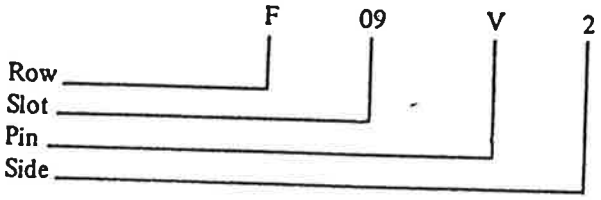
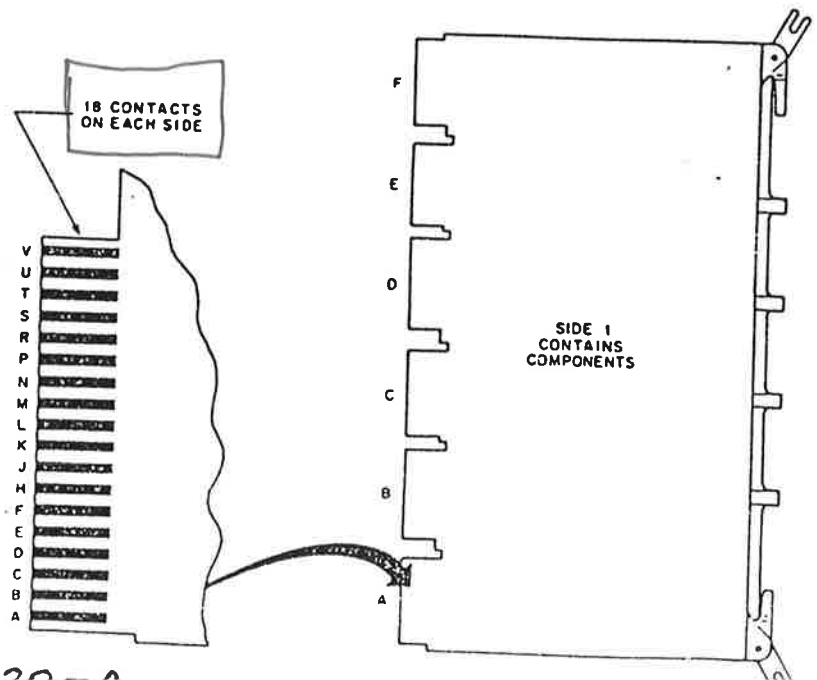


Figure 1-3 Computer Backplane Connector and Pin Designations

Figure 1-3 shows the backplane pin layout. The slots are numbered 1 through 9 and the rows are lettered A through F. Each row is pinned to accommodate a single-height, double-sided module edge-connector. The backplane accepts single, double, quad, and hex modules. A backplane pin is identified as follows:

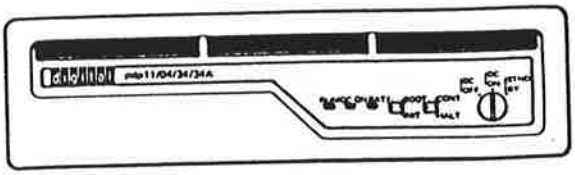


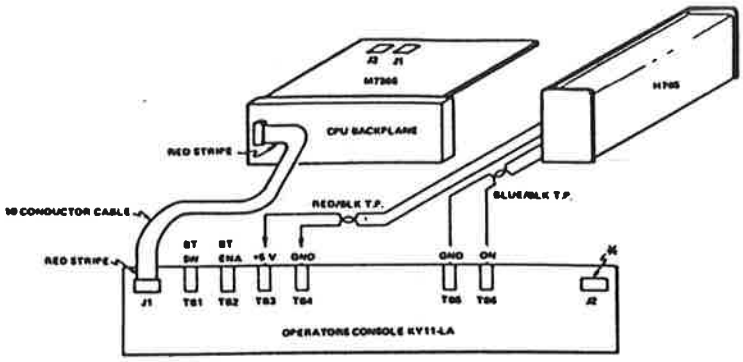
Module contact designations are shown in Figure 1-4.

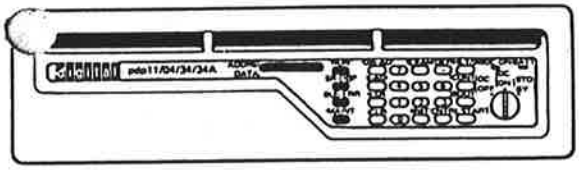


NOTES:

1. Side 1 is component side
2. Each side contains 18 contacts that are designated A-V (omitting G, I, O, Q, W, X, Y, Z)
3. A complete module contact designation contains a connector letter prefix, contact letter, and side suffix number for example AD2







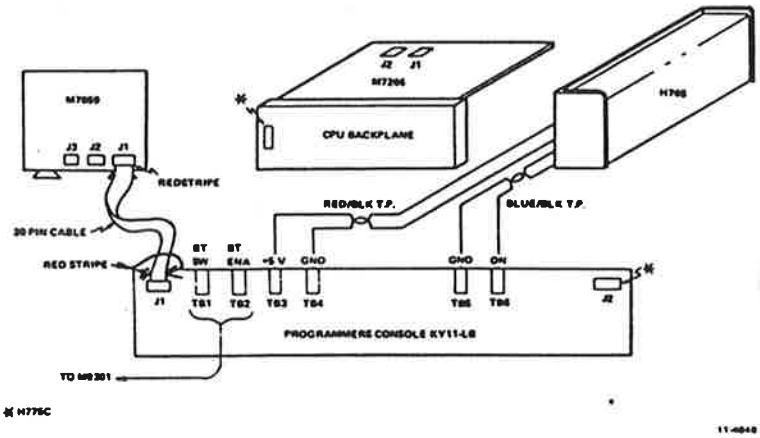
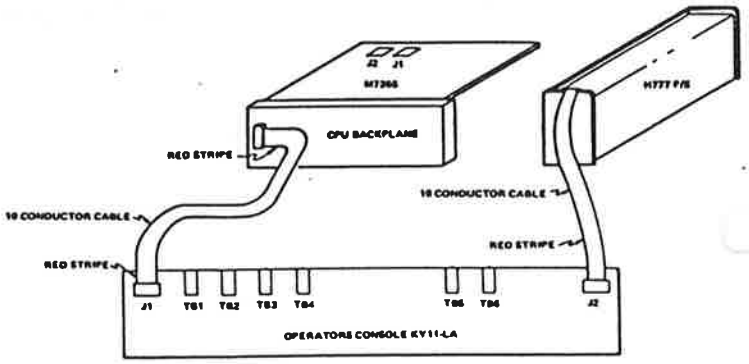


Figure 9-5 BA11-K



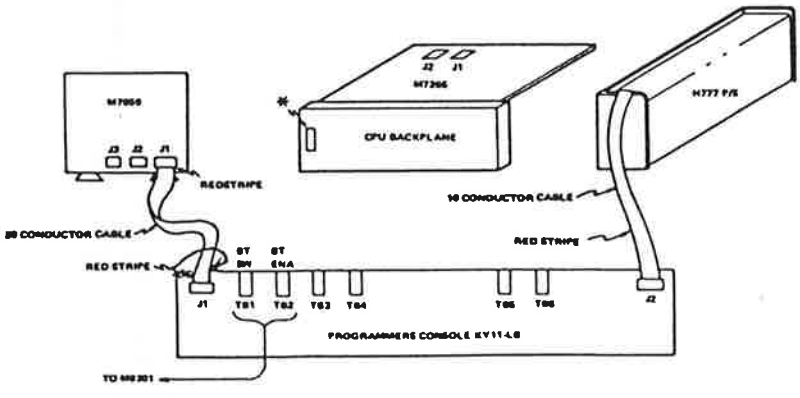


Figure 9-4 BA11-L

UNIBUS DEVICES

MODULE	DESCRIPTION	LOCATION	
M930	UNIBUS TERMINATOR	A-B 9	
M9302	UNIBUS TERMINATOR	A-B 9	WITH SACK TURNROUND
M920	UNIBUS CONNECTOR	A-B 9/AB-1	2"
M9202	UNIBUS CONNECTOR	A-B 9/AB-1	2"
M9301	BOOTSTRAP TERMINATOR	AB 3	YA-B-F
M9312	BOOTSTRAP TERMINATOR	AB 3/AB-9	
G727	GRANT CONTINUITY CARD	D 3-9	
G7274	GRANT /NPG CONTINUITY	D 3-9	

APPENDIX A
UNIBUS I/O PAGE DEVICE ADDRESSES AND VECTOR ASSIGNMENTS

Device	Address	Size in Words	Number of Devices	
AA11	776750	8	1	(first unit)
AA11	776400	8	4	(extra units)
AD01	776770	4	1	
ADF11	770460	8	1	
AFC11	772570	4	1	
AR11	770400	8	1	
BM792-YA	773000	32	1	
BM792-YB	773100	32	1	
BM792-YC	773200	32	1	
BM792-YH	773300	32	1	
BM873-YA	773000	128	1	
BM873-YB	773000	256	1	
BM873-YC	773000	256	1	
CD11	777160	4	1	
CM11	777160	4	1	
CR11	777160	4	1	
Customer	764000	1024	1	
DC11	774000	4	32	
DC14-D	777360	8	1	
Diagnostics	760000	4	1	
DL11-A	777560	4	1	(console)
DL11-A	776500	4	16	
DL11-B	777560	4	1	(console)
DL11-B	776500	4	16	
DL11-C	775610	4	31	
DL11-D	775610	4	31	
DL11-E	775610	4	31	
DL11-W	777546	1	1	(line clock, first unit only)
DL11-W	777560	4	1	(console)
DL11-W	776500	4	16	
DM11	775000	4	16	
DM11-BB	770500	4	16	(modem control for DM11)
DN11-AA	775200	4	16	
DN11-DA	775200	1	64	
DP11	774400	4	−32	(assigned backwards)
DR11-A/C	767600	4	−16	(assigned backwards)
DR11-B(1)	772410	4	1	
DR11-B(2)	772430	4	1	
DS11	775400	67	1	
DT11	777420	1	8	
DV11	775000	16	4	
DX11	776200	16	2	
Floating CSRs	760010	1020	1	
FP11	772160	8	1	
GT40	772000	4	4	
ICR/ICS11	771000	256	1	
IP11/IP300	771000	128	2	
KE11	777300	8	2	
KG11	770700	4	8	
KL11	776500	4	16	
KL11	777560	4	1	(console)
KT11	772200	64	1	
KT11-SR3	772516	1	1	
KU116-AA	777540	1	1	
KW11-L	777546	1	1	
KW11-P	772540	4	1	
KW11-W	772400	4	1	
LP11	777514	2	1	(LP0)
LP11	764004	2	1	(LP1)
LP11	764014	2	1	(LP2)
LP11	764024	2	1	(LP3)
LP11	764034	2	1	(LP4)
LP11	764044	2	1	(LP5)
LP11	764054	2	1	(LP6)
LP11	764064	2	1	(LP7)
LP20	775400	32	2	
LPA11-K	770460	8	1	
LPS11	770400	16	1	
LS11	777514	2	1	
LV11	777514	2	1	
M792	773000	32	8	
M9301-XX	765000	256	1	
M9301-XX	773000	256	1	
MM11-LP	772100	1	16	
MR11-DB	773100	64	1	
MS11-K	772100	1	16	
MS11-LP	772100	1	16	
NCV11	772760	8	1	
OST	772500	6	1	
PA611_readers	772600	32	1	(2 per PA611)
PA611_punches	772700	32	1	(2 per PA611)
PC11	777550	4	1	
PDP-11/04	777570	68	1	
PDP-11/05	777570	68	1	
PDP-11/10	777570	68	1	
PDP-11/15	777570	68	1	
PDP-11/20	777570	68	1	
PDP-11/24	777570	68	1	
PDP-11/34A	777570	68	1	
PDP-11/35	777570	68	1	
PDP-11/40	777570	68	1	
PDP-11/44	777570	68	1	
PDP-11/45	777570	68	1	
PDP-11/55	777570	68	1	
PDP-11/60	777570	68	1	
PDP-11/70	777570	68	1	
PR11	777550	4	1	
RC11	777440	8	1	
Reserved	770100	32	1	
Reserved	770440	8	1	
Reserved	772150	4	1	
Reserved	772420	4	1	
Reserved	772514	1	1	
Reserved	772550	8	1	
Reserved	775606	1	1	
Reserved	777000	56	1	
Reserved	777200	32	1	
Reserved	777510	2	1	
Reserved	777520	4	1	
Reserved	777540	3	1	
RF11	777460	8	1	
RH70/11_alt	776300	32	1	(Alternate RS/RP/RM/TJ)
RK611	777440	16	1	
RK11	777400	8	1	
RL11	774400	4	1	
RM03/04/05	776700	22	1	(RH70/RH11)
RP04/05/06	776700	22	1	(RH70/RH11)
RP11	776700	16	1	(RH70/RH11)
RS04	772040	16	1	(RH70/RH11)
RX11/RX211	777170	4	1	
TA11/DIP11-A	777500	4	1	
TC11	777340	8	1	
Testers	770000	32	1	
TM11/TMB11	772520	8	1	
TR79	764000	4	1	
TS11	772520	2	4	
TU16/45/77	772440	16	1	(RH70/RH11)
TU58	776500	4	4	
UDC-Units	771000	1	256	
UDC11	771774	2	1	
UET	772140	4	1	
Unibus-Map	770200	64	1	
VSV11	772000	4	4	
VT48	772000	16	1	
VTV01	772600	112	2	
XY11	777530	4	1	

PDP-11 INTERRUPT AND TRAP VECTORS

000	PDP-11 Reserved
004	PDP-11 CPU Errors (Illegal Instructions, Bus Errors, Stack Limit, Illegal Internal Address, Microbreak)
010	PDP-11 Reserved Instructions
014	PDP-11 Breakpoint/Trace traps
020	PDP-11 IOT Trap
024	PDP-11 Power Fail
030	PDP-11 EMT Trap
034	PDP-11 TRAP Trap
040	Reserved for System Software
044	Reserved for System Software
050	Reserved for System Software
054	Reserved for System Software
060	DL11(1), KL11(1)
064	DL11(1), KL11(1)
070	PC11, paper tape reader
074	PC11, paper tape punch
100	KW11-L, line clock
104	KW11-P, programmable clock
110	Reserved for System Software
114	CPU
120	XY11, Plotter
124	DR11-B, DMA interface
130	AD01, A/D subsystem
134	AFC11, analog subsystem
140	AA11, display
144	AA11, RSTS/E (crash-dump)
150	alternate RS/RP/RM/TJ
154	UNUSED - Reserved for Digital
160	RL11, disk
164	UNUSED - Reserved for Digital
170	LP/LS/LV11 (#1), USER RESERVED
174	LP/LS/LV11 (#2), USER RESERVED
200	LP/LS/LV11 (#0), LP20 (1), lineprinter
204	RF11, RS03/04 (RH11/RH70), MASSBUS fixed head disk
210	LP20(2), RC11, RK611/RK711
214	TC11, DECtape
220	RK11, disk
224	TM11, TS11, TU16/45, TE16, TU77, MASSBUS Magnetic tape
230	CD11, CM11, CR11
234	ICS/ICR11, IP11/IP300, UDC11
240	PDP-11-PIRQ
244	Floating Point exception
250	Memory Management error
254	RM02/03/50 (RH11/RH70), RP04/5/6 (RH11/RH70), RP11
260	DIP11, TA11
264	RX11, floppy disk
270	LP/LS/LV11 (#3), USER RESERVED
274	LP/LS/LV11 (#4), USER RESERVED
300	Floating Vectors

FLOATING CSR ADDRESS DEVICES

There is a floating address convention used for communications and other devices interfacing with the PDP-11. These addresses are assigned in order starting at 760 010 and proceeding upwards to 763 776. Floating addresses are assigned in the following sequence:

Rank	Option	Decimal Size (words)	Octal Modulus (address)
1	DJ11	4	10
2	DH11	8	20
3	DQ11	4	10
4	DU11	4	10
5	DUP11	4	10
6	LK11A	4	10
7	DMC11/DMR11	4	10 (DMC before DMR)
8	DZ11[1] and DZV11	4	10
9	KMC11	4	10
10	LPP11	4	10
11	VMV21	4	10
12	VMV31	8	20
13	DWR70	4	10
14	RL11 and RLV11	4	10 (extra only)
15	LPA11-K	8	20 (extra only)
16	KW11-C	4	10
17	Reserved	4	10
18	RX11	4	10 (extra only)
19	DR11-W	4	10
20	DR11-B	4	10 (after second)

1 DZ11E and DZ11F are dual DZ11s and are treated by the algorithm as two DZ11s

FLOATING VECTORS

There is a floating vector convention used for communications and other devices that interface with the PDP-11. These vector addresses are assigned in order starting at 300 and proceeding upwards to 777. The following Table shows the assigned sequence. It can be seen that the first vector address, 300, is assigned to the first DC11 in the system. If another DC11 is used, it would then be assigned vector address 310, etc. When the vector addresses have been assigned for all the DC11s (up to a maximum of 32), addresses are then assigned consecutively to each unit of the next highest-ranked device (KL11 or DP11 or DM11, etc.), then to the other devices in accordance with the priority ranking.

Priority Ranking for Floating Vectors

(starting at 300 and proceeding upwards)

Rank	Option	Decimal Size (words)	Octal Modulus (address)
1	DC11	4	10
1	TU58	4	10 (See Note 1)
2	KL11(extra)	4	10
2	DL11-A(extra)	4	10
2	DL11-B(extra)	4	10
3	DP11	4	10
4	DM11-A	4	10
5	DN11	2	4
6	DM11-BB	2	4
7	DH11 modem control	2	4
8	DR11-A	4	10
9	DR11-C	4	10
10	PA611(reader+punch)	8	10
11	LPD11	4	10
12	DT11	4	10
13	DX11	4	10
14	DL11-C	4	10
14	DL11-D	4	10
14	DL11-E	4	10
15	DJ11	4	10
16	DH11	4	10
17	GT40	8	10
17	VSV11	8	10
18	LPS11	12	10
19	DQ11	4	10
20	KW11-W	4	10
21	DU11	4	10
22	DUP11	4	10
23	DV11+modem control	6	10
24	LK11-A	4	10
25	DWUN	4	10
26	DMC11	4	10
26	DMR11	4	10 (DMC before DMR)
27	DZ11	4	10
28	KMC11	4	10
29	LPP11	4	10
30	VMV21	4	10
31	VMV31	4	10
32	VTV01	4	10
33	DWR70	4	10
34	RL11/RLV11	2	4 (after the first)
35	RX02	2	4
36	TS11	2	4 (after the first)
37	LPA11-K	4	10
38	IP11/IP300	2	4
39	KW11-C	4	10
40	RX11	2	4 (after the first)
41	DR11-W	2	4
42	DR11-B	2	4 (after the first)

1 There is no standard configuration for systems with both DC11 and TU58.

SECTION 2

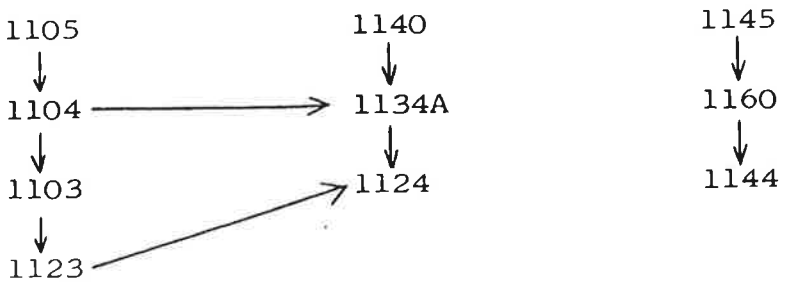
THE PDP11 FAMILY

original equipment manufactured

	O.E.M.	END USER	
1970	1115	1120	: First unibus device; Random logic C.P.U. (7 processor PCB's): 28KW of Memory.
1972	1105	1110	: Microprogrammed CPU : 32KW memory (2 processor PCB's) TTY I/O on board.
1972	1145		: Prefetched instructions : F.P.P. 128KW Memory (no M.M.).
1972	1155		: Basic 1145 with MOS + FPP (fast fortran M/C).
1974	1135	1140	: Microprogrammed CPU (less Powerfull than the 1145 - but cheaper). M.M. EIS + FPP optional extras. 5 processor PCB's. 4 optional FPP:EIS etc.
	1104		: re-engineered 1105 : No front panel (single CPU PCB) 28KW Memory.
	1134		: re-engineered 1140 - Control + Data Paths (two CPU PCB's) 128KW Memory.
	1134A		: As 1134 but allowing F.P.P. and cach options.
1975	1170		: Large powerfull mini 2MB of Memory (Massbus).
1976	LSI1103		: Chip Set (Microprocessor) implemented on a single PCB (heathKit H11) Q Bus.
1977	LSI1123		: re-engineered 1134 Control + Data Paths on a single LSI chip memory management and F.P.P. are LSI chip options.
1977	1160		: Writable control stored 128KW. → kunnen eigen instructies meegemaakt worden.
1978	1144		: re-engineered 1145 - Large mini F.P.P. MMU cach etc 2MW of memory. EUB Extended Unibus 18 Physical → 22 bit = EUB
1979	1124		: re-engineered 1134A 1123 chip set single board unibus processor. 2MW of memory.

VAX 11/780 : 4 Gigabytes

VAX 11/750



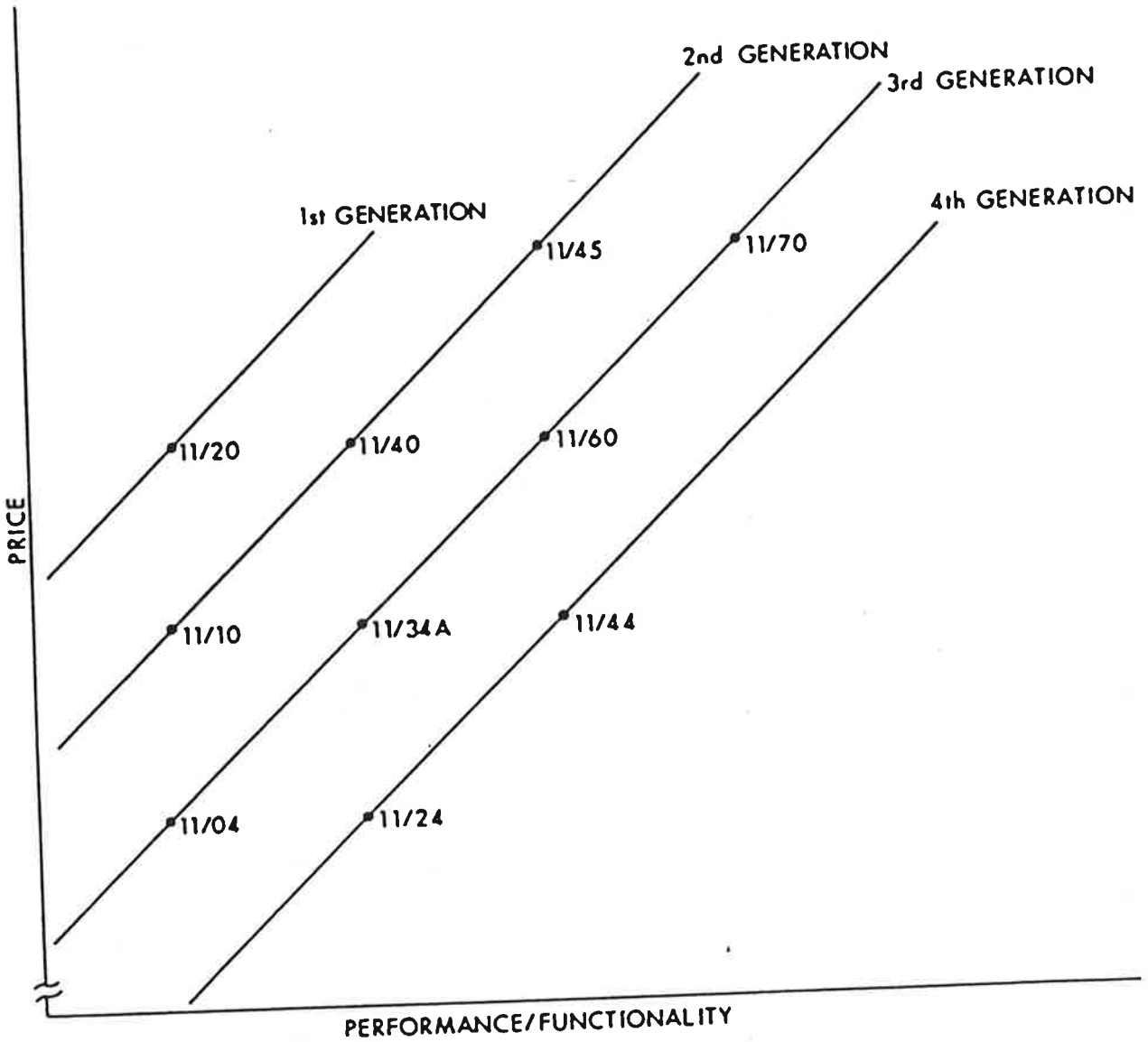


Figure 1-3 PDP-11 Performance/Functionality vs. Price

PDP 1105/10

The 1105/10 is a two pcb cpu set, comprising of Control and Data path Modules. The Data Paths has on board Line Time Clock (KW11-L) and Serial Line unit (DL11).

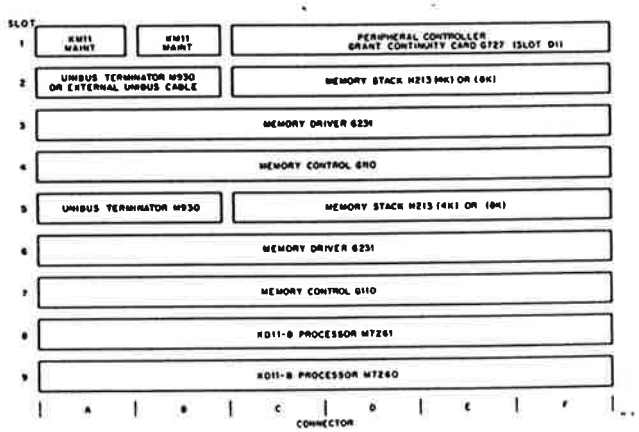
There is no Memory Management option, MAX Memory Size is 28kw.

DEVICE MNEMONIC	MODULE	DESCRIPTION	BIN
KD11-B	M 7260	Data Paths	20671
"	M 7261	Control Module	20672

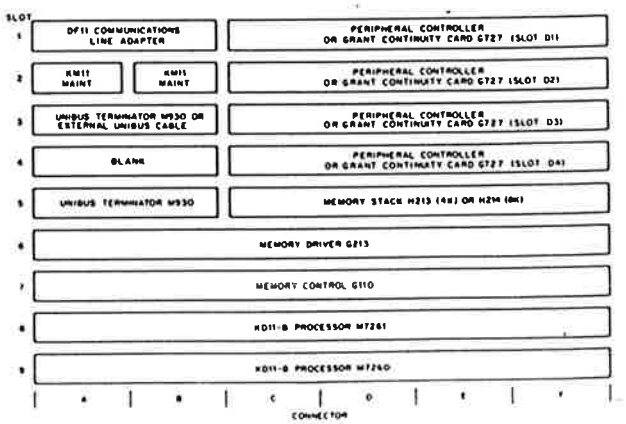
NB There are four different versions of backplanes in use. Refer to DECaid ProcA05 (1105/40/45 PSG), for maintenance information and PCB location.

Diagnostics:		
	ZQKC	PDP 11 instruction Test
	ZQKB	Systems Test
	ZKAQ	Power Fail

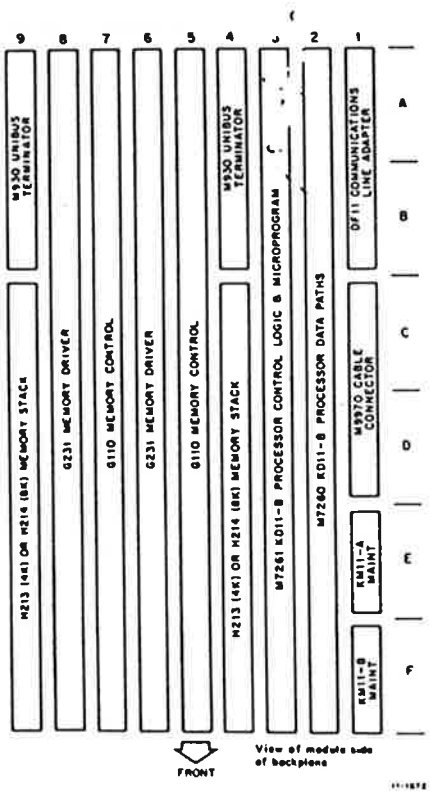
PDP-11/05-JA MODULE UTILIZATION (16K)



PDP-11/05-LA MODULE UTILIZATION (8K)



PDP-11/05-N MODULE UTILIZATION (10-1/2-Inch Mounting Box)



1135/40

The PDP 11/35 and 11/40 are system-level computers that allow increased memory expansion, memory relocation and protection, faster processing speeds and special hardware options for more powerfull operation.

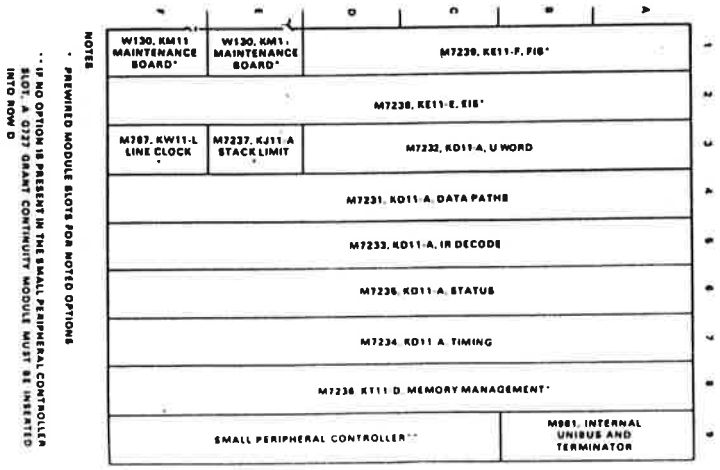
MNEMONIC	MODULE	BIN	DESCRIPTION
KD11-A	M7231	8940	Data Paths
KD11-A	M7232	8941	Microword
KD11-A	M7233	8937	IR Decode
KD11-A	M7234	8938	Timing
KD11-A	M7235	8939	Status
KT11-D	M7236	31205	Memory Management
KJ11-A	M7237	21565	Stack Limit
KE11-E	M7238	31300	Extended Instruction Set
KE11-F	M7239	31207	Floating Point

NB

Refer to PROC A40 (1105/40/45 P.S.G.) for module utilization and maintenance information.

Diagnostics

ZKAQ	Powerfail
BQEA	CPU Test
BKDM	Traps Test
BKEA	Extended Instruction Test
BKEB	
BKTA	
" B	
" C	Memory Management Test
" D	
" F	
" G	



Similar to 1140 but with Memory Management EIS and floating point as standard. Faster (300 ns) access time, 16 general registers and 3 programme modes (Kernel: Supervisor: User)

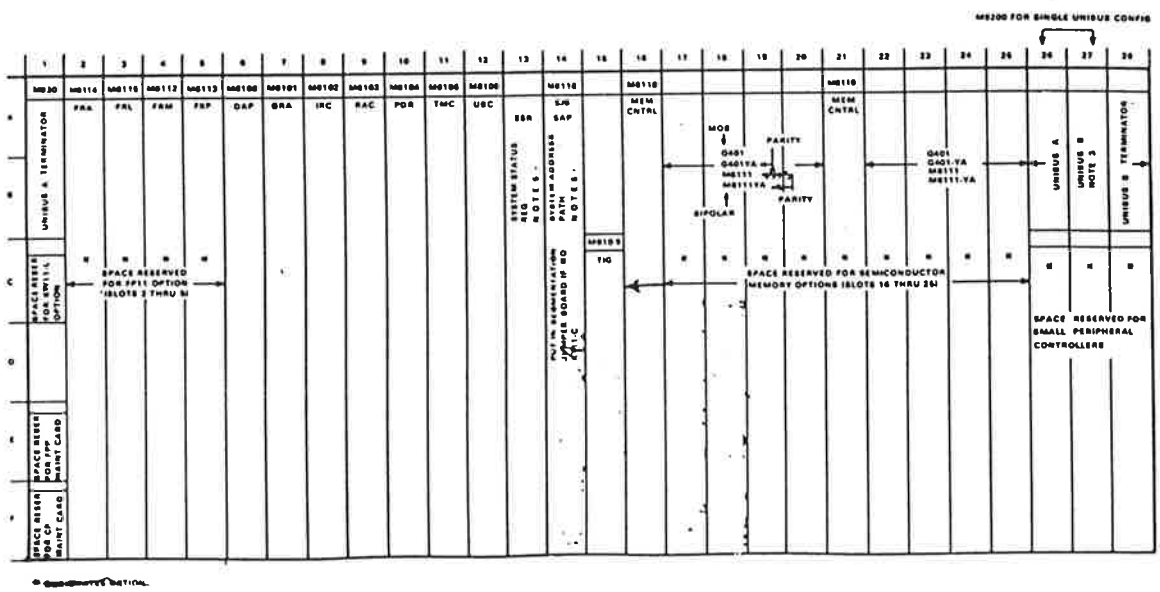
NB Uses Dedicated 28 slot Backplane, check on module positions

MNEMONIC	MODULE	BIN	DESCRIPTION
	M 8100	30190	Data Path's
	M 8101	30193	General Register Address
	M 8102	30195	Instruction Register Control
	M 8103	30200	Rom Address Control
	M 8104	30199	Proc. Data and Unibus Register
	M 8105	30226	Timing and Misc. Control
	M 8106	30227	Unibus Control
	M 8107	31392	Segmentation Address Path
	M 8108	31393	" Status Register
	M 8109	30219	Timing Generator
	M 8110		Memory Control (MOS)
	M 8111		1k x 16 bit Memory
	M 8112		FP Rom Control
	M 8113		FP Data Paths
	M 8114		Fraction High Data Paths
	M 8115		" Low " "
	M 8116	30218	Segmentation Jumper Board

Diagnostics:

CFP???	Floating Point
CKT???	Memory Management
CQKA-C	CPU
CKB???	EIS

PDP-11/45 MODULE UTILIZATION



PDP 1104

The PDP 1104 is a reengineered 1105, utilising a single hex height processor PCB, installed in a DD11-CK or Pk backplane.

The 1104 has no memory managemnet unit and therefore can only access 28kw of memory.

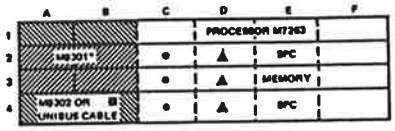
Can be used with KY11-LA operators consol or:-
KY11-LB Programmers Consol (M7859)

Mnmonic	Module	Description	Bin
KD11-D	M7263	1104 Processor	27390

Diagnostics

GKAA	Basic Instruction Test
GKAB	Interrupts and Traps Test

DD11-CK



1134

The PDP 11/34 is basically a re-engineered 1140 into a two PCB CPU. (Data paths and control) Complete with on board memory management (KT) and EIS (KE).

The PDP 11 04/34/34A use a nine slot backplane. DD11-PK (Slots 1 and 2 dedicated to the CPU boards).

Device Mnemonic	Module	Description	Bin
KD11-E	M7265	Data Paths	24058
Kd11-E	M7266	Control	24057
	*M8264	No sack To..	24059

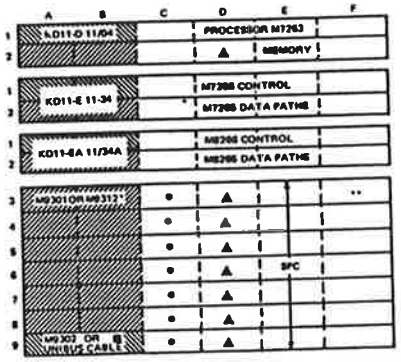
*The 1134 requires a no sack time out PCB to be installed in slot 3 spc.

The 1134 processor does not support floating point or CACH options.

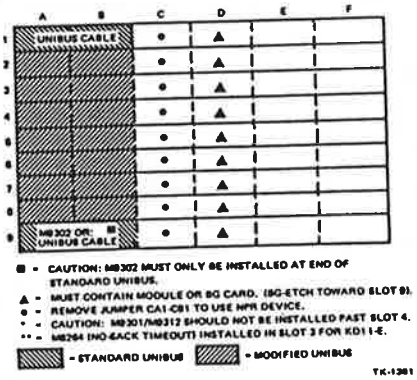
Mounting: BA11-L 5¼" Box
BA11-K 10½" Box 25A PSU

Diagnostics: See 1134A

DD11-PK



DD11-DK (expander backplane)



1134A

The PDP 1134A is a re-engineered 1134 with extra firmware to support floating point and cach options, together with circuitry to support no sack time out.

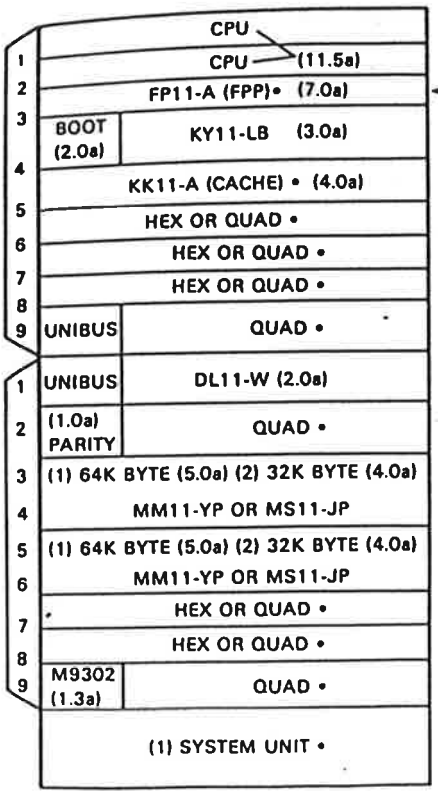
Mnemonic	Module	Description	Bin
KD11-EA	M8265	Data Paths	27617
KD11-EA	M8266	Control	27618
FP11	M8267	Floating Point	27317
KK11	M8268	Cach memory	31402

Mounting: BA11-L 5¼"
BA11-K 32A PSU

Diagnostics:

FKAA??	Basic instruction test
FKAB	Interrupts and Traps Test
FKAC	Extended instruction Tests
FKTG FKTH	Memory Management
FFPA FFPB	Floating Point
FFPC FKKA	Cach Memory

In extreme fault conditions 1134 and 1134A processor sets can be intermixed with no detriment to the user. This configuration would preclude the use of floating point and cach options.



NOTES:

1. IF THE FP11-A IS NOT USED, THE 7.0a MAY BE USED FOR 64KW of MS11-JP PARITY MEMORY OR 32KW OF MM11-YP PARITY CORE MEMORY IN SLOTS 6, 7, AND 8.
2. IF THE FP11-A IS USED, AN ADDITIONAL DD11-DK IS REQUIRED FOR ALL MEMORY DUE TO THE POWER RESTRICTIONS IN THE FIRST 9-SLOT BACKPLANE.
3. BEFORE PLUGGING IN ANY ADDITIONAL INTERFACES INTO THE EMPTY SLOTS IN THE CPU BACKPLANE, PLEASE DO A POWER CONSUMPTION CHECK IN ORDER TO ENSURE THAT THE 32 AMP POWER REGULATOR LIMIT FOR THAT CPU BACKPLANE HAS NOT BEEN EXCEEDED.

MA-2279

PDP 1124

The PDP 1124 is a redesigned 1134 utilising the 1123 LSI chip set.

The 1124 CPU is a single hex height PCB with on board serial line units (X2) and line time clock.

The 1124 utilises the E.U.B. (22 bits) giving a memory access capability of 1 mb (512 kw) of MOS memory.

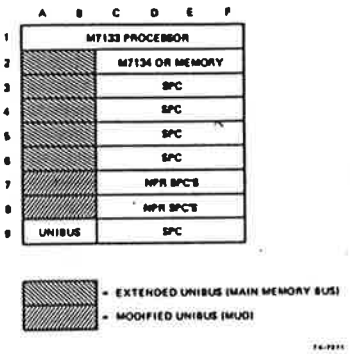
NB: To access more than 128kw the unibus map option must be installed.

Mnemonic	Module	Description	Bin
KDF11-UA	M7133	1124 CPU	39643
Options			
KT24	M7134	Unibus Map	39648
KEF11-A	LSI Chip	Floating Point	
KEF11-B	LSI Chip	Commercial Instruction	
SLU1 Address		17777560	60
SLU2 Address		17776500	300

Diagnostics

JKDA - Memory Management
JKDB - CPU
JKDC } Floating Point
JKDD }
JKDE Systems Test
JKDF SLU's and LTC
JKDH C.I.S.
KKUA Unibus Map KT24

N.B. Refer to PDP 1124 Pocket Service Guide for Maintenance information.



CPU Backplane

PDP1144

The PDP1144 is a medium scale general purpose computer with the following features:-

- Cache memory organization to provide very fast program execution speed and high system throughput
- Extended Instruction Set (EIS) for faster integer arithmetic execution
- Memory management for relocation and protection in multiuser, multitask environments
- Intelligent ASCII console with which the user can operate the computer without requiring access to the front panel
- TU58 cartridge tape interface port to make it easier to load software patches or Field Service diagnostic programs
- Ability to access up to 1 million bytes of main memory (1 byte = 8 bits) provides ample memory space for application programs
- Real-time clock which provides KW11-L compatible line-frequency clock
- 256 Kbyte ECC MOS main memory modules provide high-density, low-cost memories with error correcting codes to insure better memory reliability
- Integral DL11-W serial line unit capability
- Optional remote diagnosis
- Optional KE44A Commercial Instruction Set for faster COBOL execution
- Optional FP11-F Floating Point Processor with advanced features, operating with 32-bit and 64-bit numbers for faster FORTRAN or BASIC execution

Mnemonic	Module	Description	Bin
KD11-Z	M7090	Consol Interface Module	37688
	M7094	Data Paths	37689
	M7095	Control	37675
	M7096	Multi Function Module	37690
	M7098	Unibus Interface	37692
KK11-B	M7097	Cache Memory	37691
FP11-F	M7093	Floating Point	38950
KE11-A	M7091	Commercial Instruction Set	41207
	M7092	" " "	41206

PDP-11/44 MAINDEC DIAGNOSTICS

NOTE
Items should be executed in the order they are listed.

1.	KKFA??	11/44 Diagnostic ROM*
2.	KKAA??	11/44 CPU/EIS
3.	KKAB??	11/44 Traps
4.	KKTA??	11/44 Memory Management, Part A
5.	KKTB??	11/44 Memory Management, Part B
6.	ZM9B??	M9312/11/44 UBI Boot
7.	KKUA??	11/44 UBI MAP
8.	KKKA??	11/44 KK11-B Cache
9.	ZMSD??	MS11/M/L Memory
10.	ZDLD??	DL11-W/11/44 MFM SLU
11.	KKAC??	11/44 Power Fail
12.	KFPA??	FP11-F, Part A
13.	KFPB??	FP11-F, Part B
14	KFPC??	FP11-F, Part C
15.	ZKEE??	PDP-11 CIS Instruction Exerciser
16.	ZKUA??	UNIBUS Systems Exerciser
17	ZKUB??	UNIBUS Exerciser Module

* Diagnostic ROM is on the M7098 module

KD11-Z PROCESSOR BACK PLANE

	A	B	C	D	E	F
1	CIM ▲ M7090		CIS	M7091		
2			CIS	M7092		
3			FP	M7093		
4			DATA PATHS	M7094		
5			CONTROL	M7095		
6			MFM	M7096		
7			CACHE	M7097		
8			UBI	M7098		
9			MS11-M	M8722		
10			MS11-M	M8722		
11			MS11-M	M8722		
12			MS11-M	M8722		
13			SPC* ■			
14	M9302 OR UNIBUS CABLE		SPC* ■			

* MUST CONTAIN MODULE OR BG CARD

■ REMOVE JUMPER CA1–CB1 TO USE NPR DEVICE

▲ CAUTION DO NOT PLACE A MULTI-LAYER EXTENDER BOARD IN ROWS A & B OF SLOT #1

Module Utilization

PDP-11/60 HARDWARE

The following equipment is included as an integral part of the basic PDP-11/60 computer:

- KD11-K PROCESSOR
- 2K BYTE CACHE MEMORY (K = 1024)
- EXTENDED INSTRUCTION SET (EIS) - MUL, DIV, ASH, ASHC
- FLOATING POINT INSTRUCTION SET (FP11-C EQUIVALENT INSTRUCTIONS)
- POWER FAIL/AUTO RESTART
- HARDWARE MEMORY MANAGMENT (KT11-D EQUIVALENT)
- MEMORY IN 64K BYTE INCREMENTS OF ECC MOS OR PARITY CORE
- BATTERY BACKUP FOR MOS VERSIONS
- LINE CLOCK AND TERMINAL CONTROLLER (DL11-W)
- MULTI-DEVICE BOOTSTRAP LOADER/SELF DIAGNOSTIC TEST
- KEYPAD/NUMERIC DISPLAY CONSOLE
- LOGIC CAGE (BA11 P) WITH POWER SUPPLY (H7420) AND REGULATORS

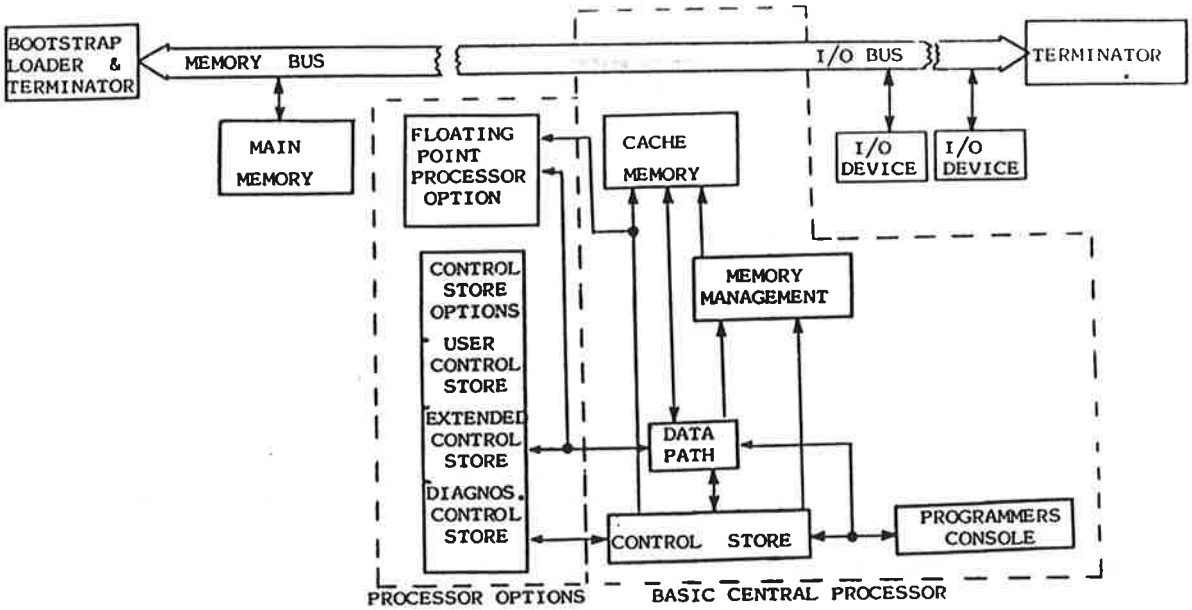
The following optional PDP-11/60 equipment is available:

- FLOATING POINT PROCESSOR (FP11-E)
- DIAGNOSTIC CONTROL STORE (FAULT ISOLATOR), KU116-BB
- USER CONTROL STORE (READ/WRITE CONTROL STORE EXTENSION), KU116-AA
- EXTENDED CONTROL STORE (READ-ONLY STORE EXTENSION), KU116/AB

11/60 PROCESSOR

There are five main diagnostics which should be run on the 11/60; these are:-

1. QKDA(AO) - KK11-K Basic Logic Test
2. QKDB(AO) - 11/60 Traps Test
3. QKDC(AO) - 11/60 CPU Exerciser
4. QKTA(AO) - 11/60 Memory Management
5. QKKA(AO) - 11/60 Cache Diagnostic



PDP-11/60 SYSTEM BLOCK DIAGRAM

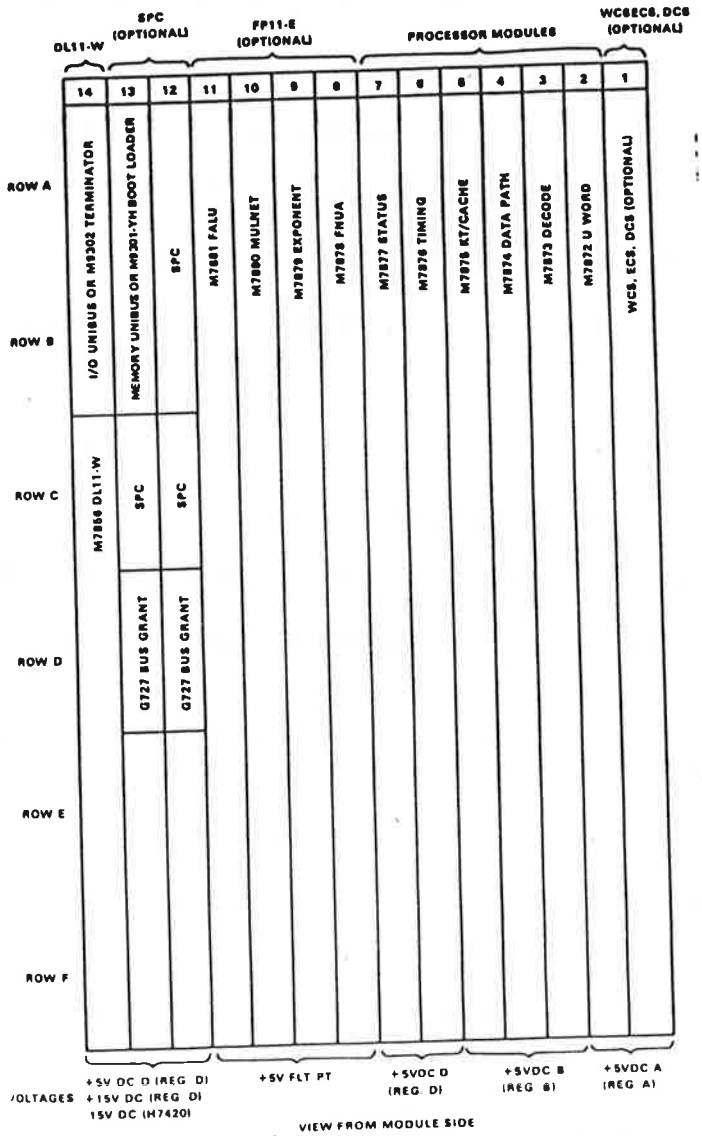


Figure 3-30 KD11-K Processor Backplane Slot and Row Assignments

PDP 11/70 FEATURES

The PDP 11/70 contains an integral part of the central processor unit, the following hardware features and expansion capabilities:

- Cache memory organization to provide very fast program execution speed and high system throughout.
- Memory managment for relocation and protection in multi-user multi-task environments.
- Ability to access up to 2 million bytes of main memory (1 Byte = 8 Bits).
- Optional high-speed, mass storage controllers as an integral part of the CPU, to provide dedicated paths to high performance storage devices.
- Optional floating point processor with advanced features and operation with 32 - bit and 64 - bit numbers.

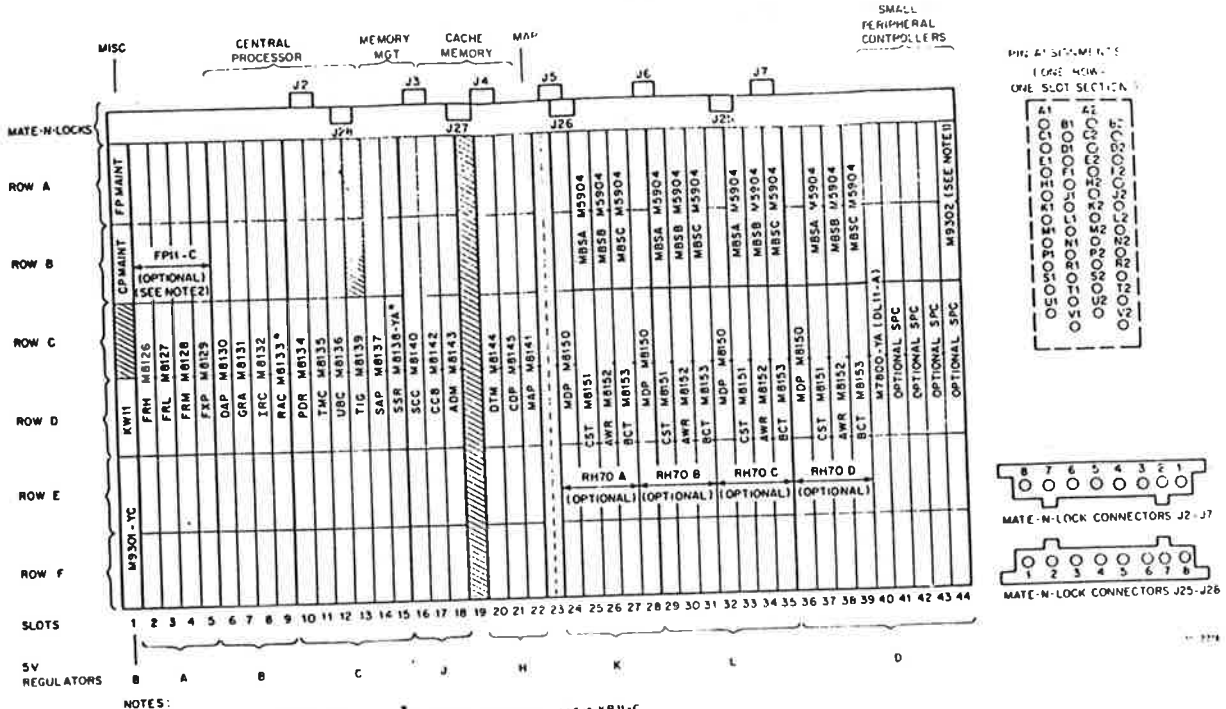
11/70 DIAGNOSTICS

General

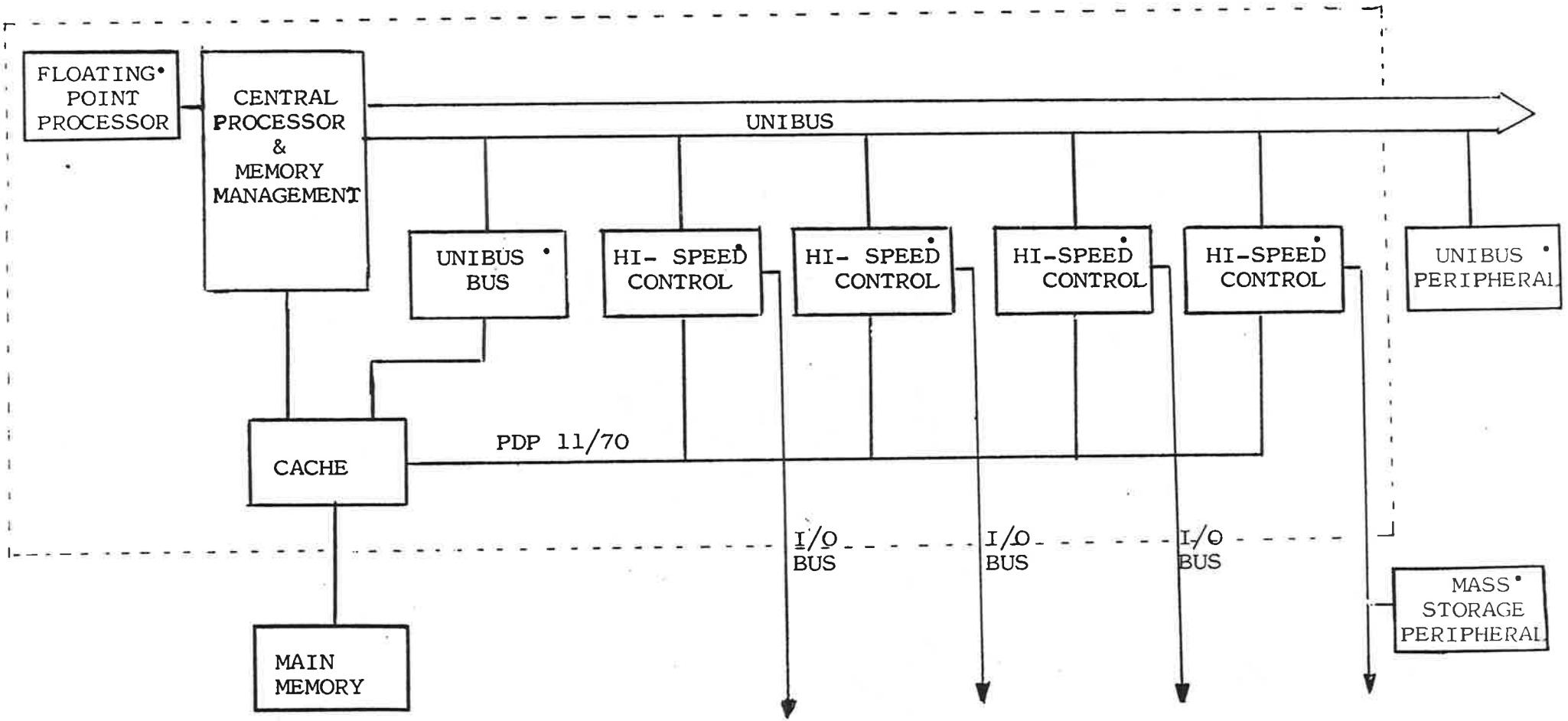
The following diagnostics are available to be run on the SYSTIME Series 6700 machine.

a) EKBABO CPU DIAGNOSTICS PART 1
b) EKBBC1 CPU DIAGNOSTICS PART 2
c) EKBCBO CACHE DIAGNOSTICS PART 1
d) EKBDCO CACHE DIAGNOSTICS PART 2
e) EKBEBO MEMORY MANAGEMENT
f) EKBFBO UNIBUS MAP DIAGNOSTICS
g) EQKCB1 CPU EXERCISER
h) EMJACO MEMORY
j) EMKAAO MEMORY
k) EFPAAO FP11-C PART 1
l) EFPBAO FP11-C PART 2

All programs should be loaded from the system disc at the OPTION stage. The diagnostics should be run in the order as listed above (a to l inclusive). Once the diagnostics are loaded into memory, load address 200 and start. If the diagnostics are successful the results will appear in the form of the following examples.



NOTES:
1 Slot 44 A,B could be UNIBUS out if there are other UNIBUS devices
2 FP-11B contains the following modules
FRH M8114
FRL M8115
FRM M8112
FXP M8113
* 3 Modules shown are used in KB11-C
KB11-B uses M8123 instead of M8123
and M8138 instead of M8138-YA



— = indicates 32-bit Data Bus
• = Optional

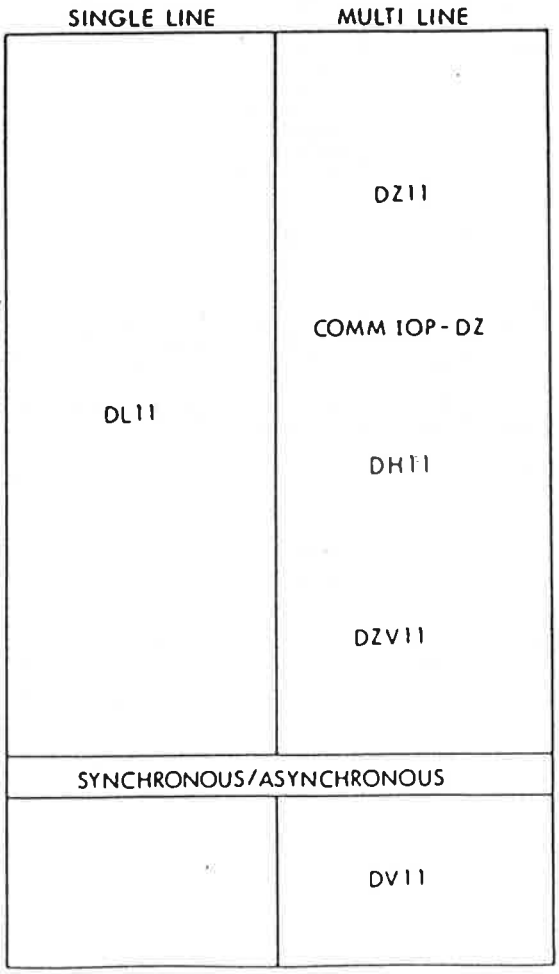
PDP-11/70 BLOCK DIAGRAM

SECTION 3

ASYNC I/O

DESCRIPTION	MODULE	MNEMONIC	LOCATION
SERIAL LINE UNIT	M7800	DL11-A-E	C-F 3-9
SERIAL LINE + LTC	M7856	DL11-W	C-F 3-8
ASYC LINE MUX. EIA	M7891	DZ11-A-B-E	A-F 3-8
ASYC LINE MUX. I.L.	M7814	DZ11-C-DOF	A-F 3-8

ASYNCHRONOUS COMMUNICATIONS INTERFACES



DL11 SERIES OF ASYNCHRONOUS LINE INTERFACES

Originally there were five available DL11 Options, DL11-A through DL11-E.

Now the DL11-W can replace DL11-A, -B, -C, and -D modules in most applications, and it is the most widely used DL11.

However, the DL11-W cannot always replace the DL11-E, which is the only version with the full control set needed with some modems.

DL11 Options

Option	Data Code	Typical Use	Baud Rates	Notes	Description
DL11-A	Restricted[1]	Model 33 or 35 Teletype Model VT05 Display Terminal	110 150 300 600 1200 2400	a. No dataset bits a. No BREAK or ERROR bits c. No 1200/110 split	Uses 20-mA current loop operation for receive, transmit, and reader run.
DL11-B	Restricted[1]	Model VT05 or VT06 Display Terminal	Same as DL11-A	a. No dataset bits b. No BREAK or ERROR bits c. No 1200/110 split d. DATA TERMINAL RDY and REQ TO SEND bits strapped on permanently e. Null modem usually required for local EIA terminal	Has EIA drivers and receivers for compatability with EIA terminals.
DL11-C	Full Selection[2]	Model 28 Teletype	Crystal and switch selectable[3]	a. No dataset bits b. BREAK and ERROR bits enabled	Basically identical to DL11-A except has full code and baud rate selection. Also includes both BREAK and ERROR bits.
DL11-D	Full Selection[2]	Model 37 Teletype (null modem required)	Crystal and switch selectable[3]	a. No dataset bits b. BREAK and ERROR bits enabled c. DATA TERMINAL RDY and REQ TO SEND bits strapped on permanently	Basically identical to DL11-B except has full code and baud rate selection. Also includes both BREAK and ERROR bits.
DL11-E	Full Selection[2]	Model 103 or 202 modems	Crystal and switch selectable[3]	a. Full dataset control	Provides complete dataset control. Dataset lines monitored by this interface are: RING, RECEIVE DATA, CARRIER DETECT, CLEAR TO SEND, and SECONDARY RECEIVE DATA. Dataset lines controlled by the program are: TRANSMITTED DATA, REQUEST TO SEND, SECONDARY TRANSMITTED DATA, and DATA TERMINAL READY.

DL 11 E

WORD STRUCTURE
DEVICE ADDRESS
VECTOR ADDRESS

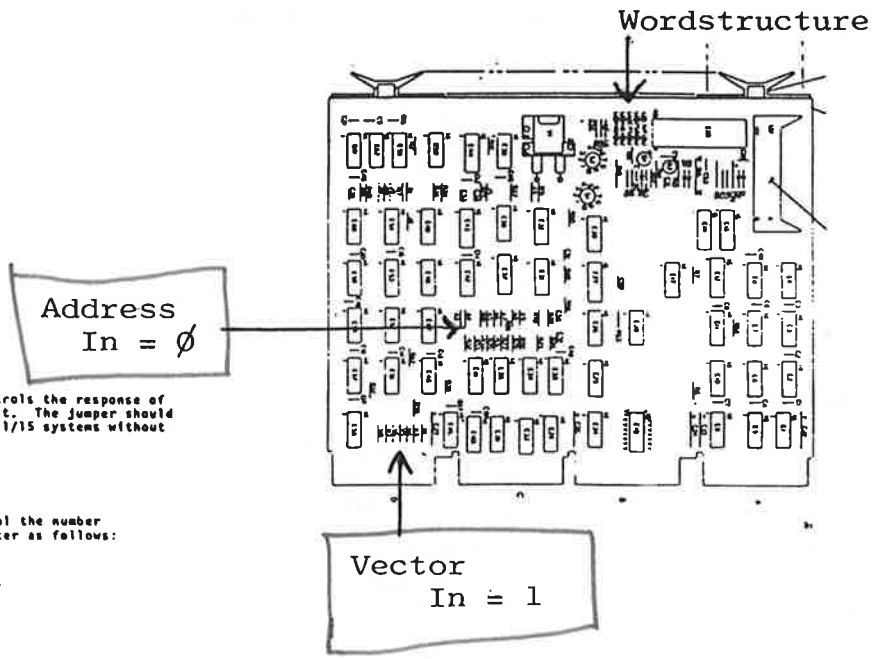
SET BY LINKS

BAUD RATE — SET BY SEPERATR TX/RX 10 POSITION ROTARY SWITCHES

NOTE — THE XTAL MUST BE REPLACED TO COVER THE COMPLETE RANGE OF BAUD RATES

CURRENT LOOP — BERG CONNECTOR H ⟶ E
~~MAKE AND LOGIC~~ CONNECTOR
MATE + LOCK

EIA — BERG CONNECTOR M ⟶ E
V24 PLUG



C. SPECIAL NPR JUMPER:

Jumper N1, shown on drawing DL-6, controls the response of the interrupt circuit to an NPR request. The jumper should normally be IN, except for 11/20 and 11/15 systems without the KN11 option.

F. SELECTION OF DATA FORMAT:

1. Data Bits

Split lug pairs NB2 and NB1 control the number of data bits in the serial character as follows:

NB2	NB1	# OF DATA BITS	
OUT	OUT	8	←
OUT	IN	7	
IN	OUT	6	
IN	IN	5	

2. Parity

Parity is controlled by split lug pairs PE and EPS as follows:

PE	EPS	PARITY	
OUT	OUT	OFF	←
OUT	IN	OFF	
IN	OUT	EVEN	
IN	IN	ODD	

3. Stop Bits

Split lug pair 2SB and jumpers J9, J10 and J11 control the number of stop bits in the serial character as follows:

2SB	J9	J10	J11	# OF STOP BITS	
OUT	OUT	IN	OUT	2	
IN	OUT	IN	OUT	1	←
IN	OUT	OUT	IN	1.5 for TI, GI, and SCM UARTS	
IN	IN	OUT	OUT	1.5 for WD UARTS	

G. CRYSTAL SELECTION:

The clocking scheme of the DL11 consists of a single crystal oscillator feeding a divider network, with two 10-position switches tapping various points to feed into the UART's

SPEED GROUP		1	2	3	4
		CRYSTAL (HZ)			
POSITION	FACTOR	844.8K	1.03296M	1.152M	4.608M
1*	23040	36.7	44.8	50	200
2	15360	55	67.3	75	300
3	7680	110	134.5	150	600
4	3840	220	269	300	1200
5	1920	440	538	600	2400
6	960	880	1076	1200	4800
7	640	1320	1614	1800	7200
8	480	1760	2152	2400	9600

*Most counter-clock wise position.

INSTALLATION OF DL 11-A-W

1) CHECK DEVICE ADDRESS 777560 = CONSOL TERMINAL

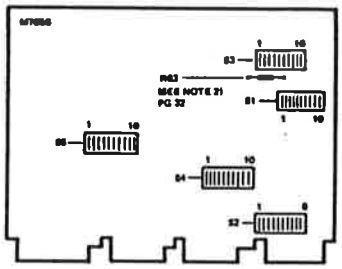
2) CHECK VECTOR ADDRESS 060

3) CHECK WORD STRUCTURE, PARITY, START/STOP bits

4) CHECK BAUD RATE

5) EIA OR CURRENT LOOP - V24/MATE AND LOCK

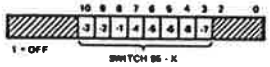
6) RUN DIAGNOSTIC ZDLD



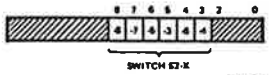
ADDRESS AND VECTOR SELECTION

For standard console device address = 777560
vector = 060

ADDRESS:
(77400X - 77777X)*



VECTOR:
(007 - 77X)*



BAUD RATE	XMIT S4-10	S3-1	S3-4
110	ON	ON	ON
150	OFF	ON	ON
300	ON	OFF	OFF
600	ON	OFF	ON
1200	ON	ON	OFF
2400	OFF	OFF	OFF
4800	OFF	OFF	ON
9600	OFF	ON	OFF

BAUD RATE	RECEIVE S3-2	S3-3	S3-5
110	OFF	OFF	OFF
150	ON	OFF	OFF
300	OFF	ON	ON
600	OFF	ON	OFF
1200	OFF	OFF	ON
2400	ON	ON	ON
4800	ON	ON	OFF
9600	ON	OFF	ON

LINE CLOCK

Address set for 777546

S5-9	S5-10	
OFF	ON	Enable (SLU and LTC)
ON	OFF	Disable (SLU only)
ON	ON	DL11-W is line clock only. SLU does not respond to any address

NOTES

1. LTC must be disabled if SLU is other than console interface.
2. When using multiple DL11-W's, only one should have LTC enabled. R63 should be removed on all

DATA FORMAT

No. Bits	S4-4	S4-3	No. Stop Bits	S4-5
5	ON	ON	1	ON
6	ON	OFF	2	OFF*
7	OFF	ON		
8	OFF	OFF		

PARITY

Enable:	S4-6 ON	Odd:	S4-2 ON
Disable:	S4-6 OFF	Even:	S4-2 OFF

TRANSMITTER

	S1-1	S1-2	S1-3	S1-6	S1-7
20 mA loop active**	ON	ON	OFF	OFF	ON
20 mA loop passive	OFF	OFF	ON	ON	OFF

RECEIVER

	S3-6	S3-7	S3-8	S3-9	S3-10
Active**	ON	OFF	ON	OFF	ON
Passive	OFF	ON	OFF	ON	OFF

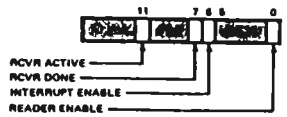
PAPER TAPE READER ENABLE

	S1-4	S1-5	S1-8	S1-9	S1-10
Active**	ON	OFF	ON	OFF	ON
Passive	OFF	ON	OFF	ON	OFF

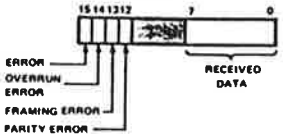
RCVR Error Bits		Break	
Enable:	S4-7 ON	Enable:	S4-1 ON
Disable:	S4-7 OFF	Disable:	S4-1 OFF

* 1 5 with five data bits
** The most common configuration is with the DL11-W active and the terminal passive.

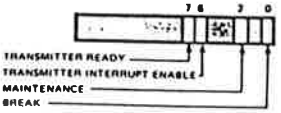
RCSR Console Address: 777560



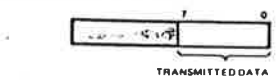
RBUF Console Address: 777562



XCSR Console Address: 777564



XBUF Console Address: 777566



LKS Console Address: 777546

DL11-W (M7856)
(address 176500, vector 300, speed 9,600 baud)

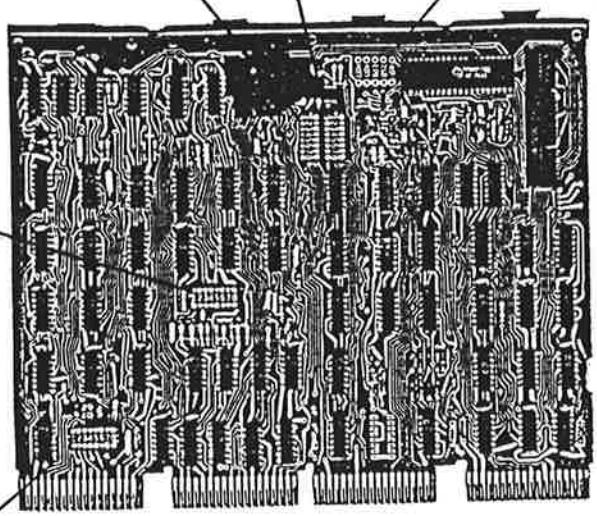
Switch Pack	Switch No.	Position
1		Not used (Switch placement unspecified)
2	1	X
	2	X
	3	OFF
	4	OFF
	5	ON
	6	OFF
	7	ON
	8	OFF
3	1	ON
	2	ON
	3	OFF
	4	OFF
	5	ON
	6-10	X
4	1	ON
	2	X
	3	OFF
	4	OFF
	5	ON
	6	OFF
	7	OFF
	8	X
	9	X
	10	OFF
5	1	OFF
	2	ON
	3	OFF
	4	ON
	5	OFF
	6	ON
	7	ON
	8	ON
	9	ON
	10	OFF

SYSTIME DL11

Functionally equivalent to DEC DL11-E - Brown Handles

All links set as per DL11-E

BIN 34381



SW	1	2	3	4	5	6	7	8
ADD	3	4	5	6	7	8	9	-

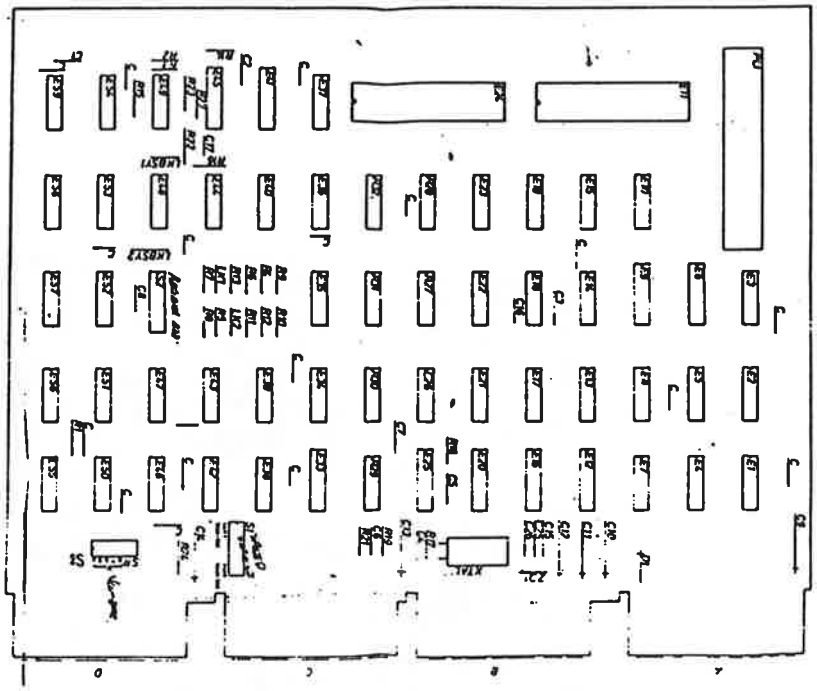
SW	1	2	3	4	5	6	7	8
VEC	8	7	6	5	4	3	-	-

BAUD RATE : SEE DL11-E TABLE

SYSTIME DUAL DL11

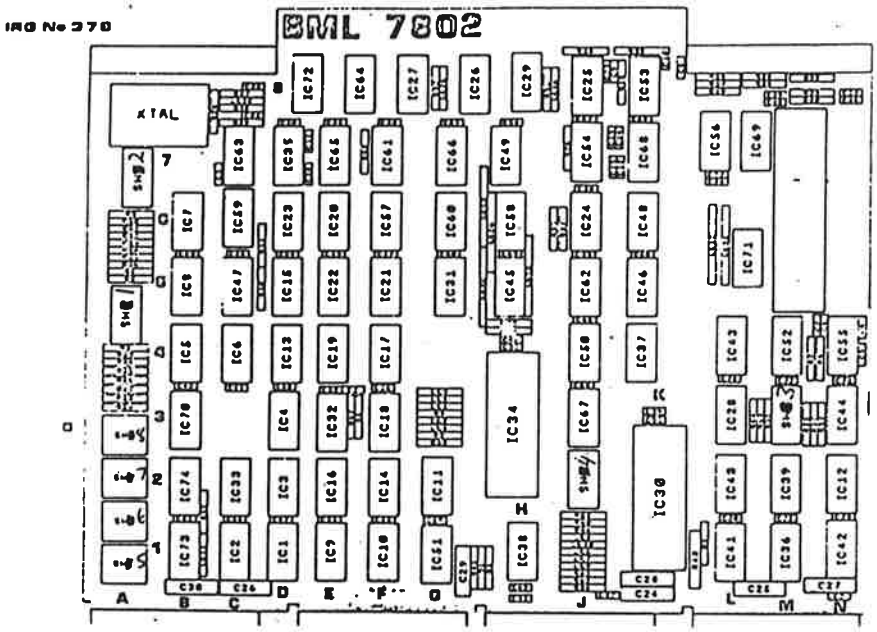
Bin 35180

Two Channel Dl11	-	Black Handles
Base ADDRESS	SW2	on=0
Base VECTOR	SW3	on=1
Baud Rate	SW1	1-4 - A 9600:1200:600:300 5-8 - B
Single Device	Link 1 out Link 2 in	



SW3	5 4 3 2 1
Vector	8 7 6 5 4
SW2	8 7 6 5 4 3 2 1
ADDRESS	10 9 8 7 6 5 4 3

DIAGNOSTICS ZDLD fails Test 32



Baud Rate Selection

Switch 5	-	Receiver Clock Channel 1
Switch 6	-	Transmitter Clock Channel 1
Switch 7	-	Receiver Clock Channel 2
Switch 8	-	Transmitter Clock Channel 2

Position 1 (fully anti-clockwise)	9600
Position 2	4800
Position 3	2400
Position 4	1200
Position 5	600
Position 6	300
Position 7	200
Position 8	150
Position 9	75
Position 10	110/134.5

Address	Channel 1	Channel 2
A10	Sw.Pk. 1 - 8	Sw.Pk. 2 - 8
A09	Sw.Pk. 1 - 7	Sw.Pk. 2 - 7
A08	Sw.Pk. 1 - 6	Sw.Pk. 2 - 6
A07	Sw.Pk. 1 - 5	Sw.Pk. 2 - 5
A06	Sw.Pk. 1 - 4	Sw.Pk. 2 - 4
A05	Sw.Pk. 1 - 3	Sw.Pk. 2 - 3
A04	Sw.Pk. 1 - 2	Sw.Pk. 2 - 2
A03	Sw.Pk. 1 - 1	Sw.Pk. 2 - 1

Switch Pack

Vector	Channel 1	Channel 2
V08	Sw.Pk. 4 - 1	Sw. Pk. 3 - 1
V07	Sw.Pk. 4 - 7	Sw. Pk. 3 - 7
V06	Sw.Pk. 4 - 6	Sw. Pk. 3 - 6
V05	Sw.Pk. 4 - 5	Sw. Pk. 3 - 5
V04	Sw.Pk. 4 - 4	Sw. Pk. 3 - 4
V03	Sw.Pk. 4 - 3	Sw. Pk. 3 - 3

The special NPR jumper, Link 11 (by Unibus connector F) should normally be IN, except for 11/20, 11/15 and 11/70 Systems without the KH11 option.

Selection of data format

Link 1 and Link 2 control the number of data bits in the serial character for Channel 1.

Link 6 and Link 7 control the number of data bits in the serial character for Channel 2.

Channel 1 Channel 2	Link 1 Link 6	Link 2 Link 7	No. of Bits
	OUT	OUT	8
	OUT	IN	7
	IN	OUT	6
	IN	IN	5

Parity is controlled by Link 3 and Link 4 for Channel 1 and Link 8 and Link 9 for Channel 2.

Channel 1 Channel 2	Link 3 Link 8	Link 4 Link 9	Parity
	OUT	OUT	NONE
	OUT	IN	NONE
	IN	OUT	EVEN
	IN	IN	ODD

The number of stop bits is controlled by Link 5 for Channel 1 and Link 10 for Channel 2.

Channel 1 Channel 2	Link 5 Link 10	No. of Stop Bits
	OUT	2
	IN	1

2

Links 12A and 21A tie the EIA driver to REQUEST TO SEND lead (pin 4) of the dataset cable on Channel 1 and Channel 2 respectively. IN for 7802-B, D and E; does not affect 7802-A and C.

Links 12B and 21B tie the EIA driver, normally used for the REQUEST TO SEND lead, to FORCE BUSY lead (pin 25) for use with Bell 103E. This is a customer option. If not specified, jumper is OUT for all 7802's.

Switch Pack 3 - 2 and Switch Pack 4 - 2 when IN, forces "DATA LEADS ONLY" mode of operation for Channel 1 and 2 respectively. Turns DATA TERMINAL READY (pin 20) and REQUEST TO SEND (pin 4) on. IN for 7802-B and D; OUT for 7802-E; does not affect 7802-A and C.

Switch Pack 3 - 8 and Switch Pack 4 - 8 when IN, allows REQUEST TO SEND lead (pin 4) to be controlled by bit 2 of the receiver status register. OUT for 7802-B and D; IN for 7802-E; does not affect 7802-A and C.

Link 16 and Link 26 when IN, allows DSET INT to cause interrupts for Channel 1 and 2 respectively. OUT for 7802-A, B, C and D; IN for 7802-E.

Links 22A/B and 23A/B control Channel 1.
Links 24A/B and 25A/B control Channel 2.
When 'A' link is inserted, allows dataset control bits to be read as part of receiver status register. When 'B' link is inserted, prevents dataset control bits from being read.

QUADRASYNC/B

The Quadrasync/B provides four asyncronous EIA serial communications channels.

INSTALLATION

The quadrasync/B is a quad size PCB which can be installed into any small peripherals slot (SPC).

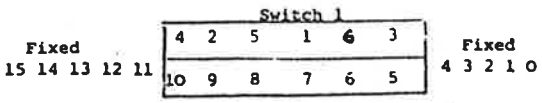
Fig 1 Address selection

Fig 2 Vector selection

Fig 3 Speed selection

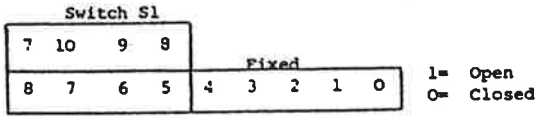
Fig 1 Address selection:

Switch 1



Open= 0
Closed= 1

Fig 2 Vector selection:



Vector address selection selects the beginning vector address for the four channels of the quad/B.

Data Rates

The quad/B offers six independant selectable baud rates for each channel. The transmitter and receiver for each channel operate at the identical baud rate. The baud rates are:

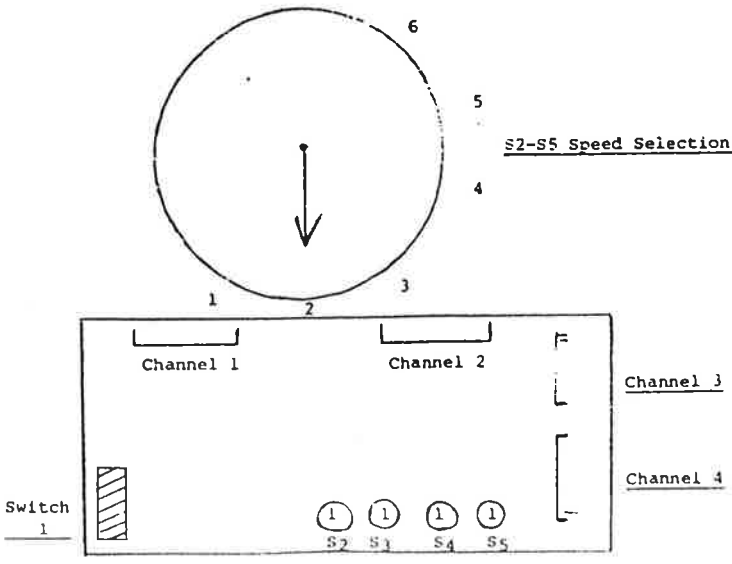
Fig 3

Baud Rate	Switch Position
9600	1
4800	2
2400	3
1200	4
600	5
300	6

Notes

1) Switch position 2 is when the arrow on the switch is pointing directly down.

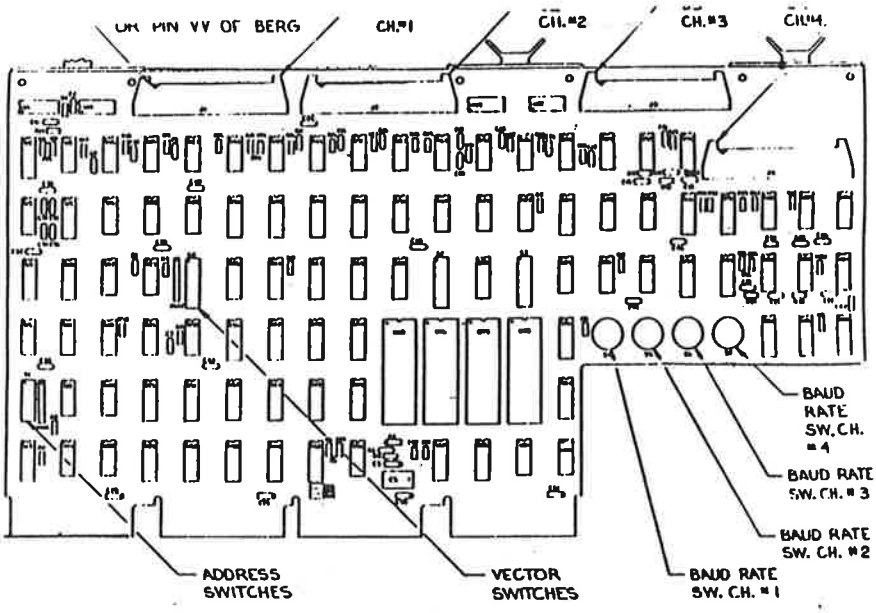
2) Ascending switch positions are in the counter clockwise direction.



Board Layout

FUNCTION

Provides an interface between the PDP*-11 Unibus* and four asynchronous EIA Serial Communication Channels with complete dataset control for each channel. System software compatible with the Digital Equipment Corporation DL-11E. (Does not support current Loop or reader enable relay circuit).



DATA RATES

The QUADRASYNC/E offers eight independently selectable baud rates for each channel. The transmitter and receiver of each channel operate at the identical baud rate. The baud rates are:

BAUD RATE	SWITCH POSITION
9600 baud	1
4800 baud	2
2400 baud	3
1200 baud	4
600 baud	5
300 baud	6
150 baud	7
75 baud	8

NOTES:

1) Switch position 1 is when the arrow ON switch is pointed directly toward the letter '1' printed on the circuit board.
2) Ascending switch positions are in clockwise direction.
3) CH 1 switch is closest to center of board and ascending to CH 4 on left side of board.

M-447

	PARITY SELECT			
CHANNEL	ENABLED	DISABLED	ODD	EVEN
1	S2-1 CLOSED	S2-1 OPEN	S2-2 CLOSED	S2-2 OPEN
2	S2-6 CLOSED	S2-6 OPEN	S2-7 CLOSED	S2-7 OPEN
3	S3-1 CLOSED	S3-1 OPEN	S3-2 CLOSED	S3-2 OPEN
4	S3-6 CLOSED	S3-6 OPEN	S3-7 CLOSED	S3-7 OPEN

	WORD LENGTH SELECT			
CHANNEL	5 DATA BITS	6 DATA BITS	7 DATA BITS	8 DATA BITS
1	S2-4 CLOSED S2-5 CLOSED	S2-4 CLOSED S2-5 OPEN	S2-4 OPEN S2-5 CLOSED	S2-4 OPEN S2-5 OPEN
2	S2-9 CLOSED S2-10 CLOSED	S2-9 CLOSED S2-10 OPEN	S2-9 OPEN S2-10 CLOSED	S2-9 OPEN S2-10 OPEN
3	S3-4 CLOSED S3-5 CLOSED	S3-4 CLOSED S3-5 OPEN	S3-4 OPEN S3-5 CLOSED	S3-4 OPEN S3-5 OPEN
4	S3-9 CLOSED S3-10 CLOSED	S3-9 CLOSED S3-10 OPEN	S3-9 OPEN S3-10 CLOSED	S3-9 OPEN S3-10 OPEN

	STOP BIT SELECT	
CHANNEL	ONE	TWO
1	S2-3 CLOSED	S2-3 OPEN
2	S2-8 CLOSED	S2-8 OPEN
3	S3-3 CLOSED	S3-3 OPEN
4	S3-8 CLOSED	S3-8 OPEN

VECTOR ADDRESS:

SWITCH 8						FIXED			VECTOR
5	6	7	8	9	10				
8	7	6	5	4	3	2	1	0	
X	X	X	X	X	X	0	0	0	RCVR
X	X	X	X	X	X	1	0	0	XMIT

SW-OPEN = 1
SW-CLOSED = 0

Vector address selection selects the beginning vector addresses for the four channels of the Quad/E.

Vector addresses are normally set to 774 thru 740

VECTOR RANGE: 000 through 777

OPERATION WITHOUT MODEM: The QUADRASYNC/E is normally used for operation with a modem. Any or all of the four QUADRASYNC/E channels can be modified for use without modem by using positions 1 through 4 of switch 8. These switches are normally set to the open position which causes the Data Terminal Ready and Request to Send signals to be under program control. For operation without modem, these two signals can be switched to the ON state. For applications with modem on some lines and not on others, a null modem can be used on the no-modem lines. The table below shows the switch settings for each channel. For applications with modem on none of the lines, close all four switches and address the device as a DL11-B.

Switch 8		Description of Setting
Position	Setting	
4	Open	Channel 1 - normal operation with modem
4	Closed	Channel 1 - operation without modem
3	Open	Channel 2 - normal operation with modem
3	Closed	Channel 2 - operation without modem
2	Open	Channel 3 - normal operation with modem
2	Closed	Channel 3 - operation without modem
1	Open	Channel 4 - normal operation with modem
1	Closed	Channel 4 - operation without modem

FIXED						SWITCH 1								FIXED			REGISTER
						1	2	3	4	5	6	7	8				
17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
1	1	1	1	1	1	1	X	X	X	X	X	X	X	X	0	0	0	RCSR
1	1	1	1	1	1	1	X	X	X	X	X	X	X	X	0	1	0	RBUF
1	1	1	1	1	1	1	X	X	X	X	X	X	X	X	1	0	0	XCSR
1	1	1	1	1	1	1	X	X	X	X	X	X	X	X	1	1	0	XBUF

Address Range: 777776 thru 774000

Address is normally set for: 775610 thru 775646

Address selection selects the beginning address of the 16 contigous address of the Quad/E

SW - OPEN = 0
SW - CLOSED = 1

3 - 9 X

SYSTIME QUAD DL11

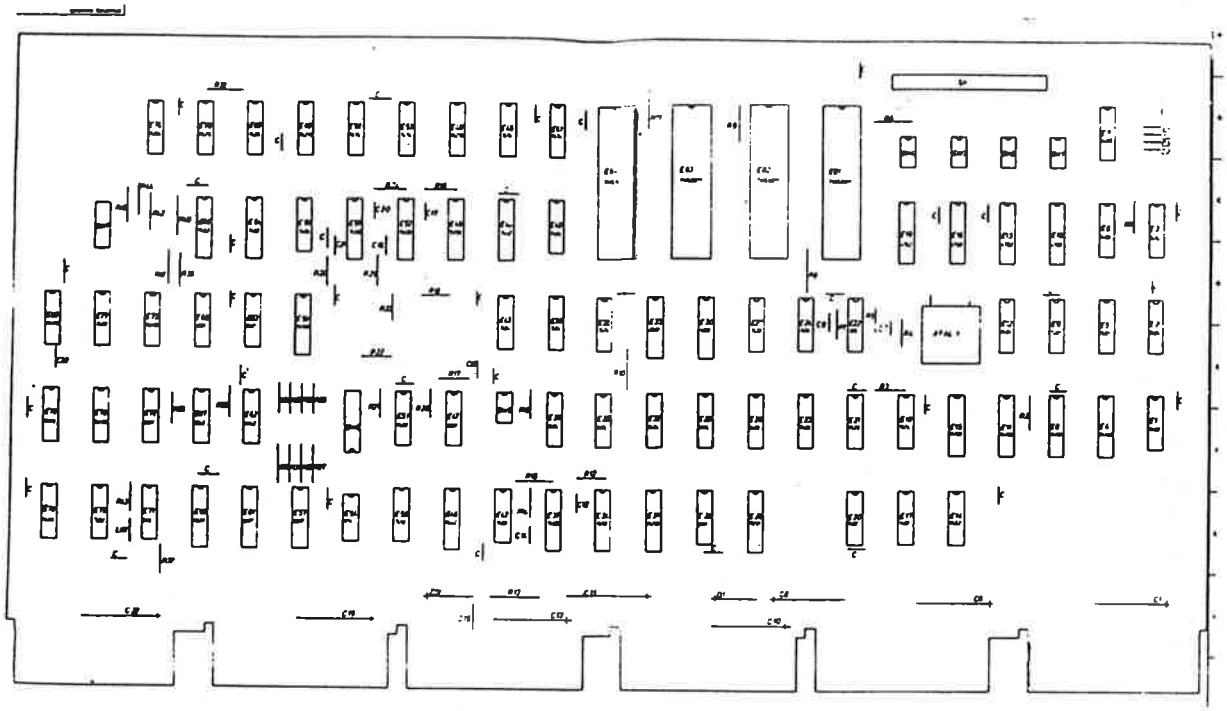
: 4 Channel DL11 - Handle: Black

Base Address: 176500 (SWKA)

Base Vector: 300

Mode: SWKB

Baud Rate: SW 1,2,3,4



NOTE 1
THREE KB MODE MUST HAVE ODD ADDRESS START 10 ABOVE BASE 00 OR 40.

NOTE 2
DUAL KB MODE ADDRESS MUST BE EVEN BASE i.e. 00, 20, 40, 60

MODE	SWKB 1	2	3	4
QUAD	OFF	OFF	OFF	OFF
THREE	OFF	ON	OFF	OFF
DUAL	ON	OFF	OFF	OFF
SINGLE	ON	OFF	ON	ON

SW4	CTØ	BAUD RATE
1	= 1	=
2	= 2	=
3	= 3	=

SKWA 10 9 8 7 6 5 4 3

ADD BIT 10 9 8 7 6 5 4 3

On = Ø

OFF = 1

BASE VECTOR	6	5	4	3	2	1
300	ON	OFF	OFF	ON	ON	ON
310	ON	OFF	OFF	ON	ON	OFF
320	ON	OFF	OFF	ON	OFF	ON
330	ON	OFF	OFF	ON	OFF	OFF
340	ON	OFF	OFF	OFF	ON	ON
350	ON	OFF	OFF	OFF	ON	OFF
360	ON	OFF	OFF	OFF	OFF	ON
370	ON	OFF	OFF	OFF	OFF	OFF
400	OFF	ON	OFF	ON	ON	ON
410	OFF	ON	ON	ON	ON	OFF
420	OFF	ON	ON	ON	OFF	ON
430	OFF	ON	ON	ON	OFF	OFF
440	OFF	ON	ON	OFF	ON	ON
450	OFF	ON	ON	OFF	ON	OFF
460	OFF	ON	ON	OFF	OFF	ON
470	OFF	ON	ON	OFF	OFF	OFF
500	OFF	ON	OFF	ON	ON	ON

VECTOR SWITCH

BASE VECTOR FOR LOWEST KB OF GROUP OFF 4

SWITCH TO OFF POSITION FOR LOGICAL '1'

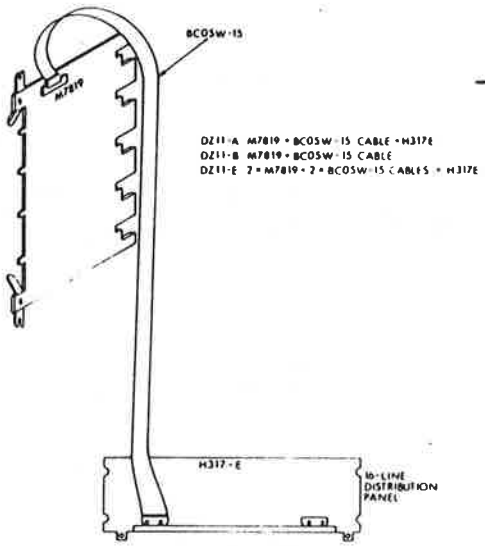
IF 3 KB MODE SET VECTOR TO 10_8 BELOW FIRST VECTOR REQUIRED

E1A M7819
11 M7814 *

A)) B)	E1A PARTIAL MODEM CONTROL	8 CHAN
E	COMBINATION OF A + B	16 CHAN
* C)) * D)	20 MA	8 CHAN
* F)	COMBINATION OF C + D	16 CHAN

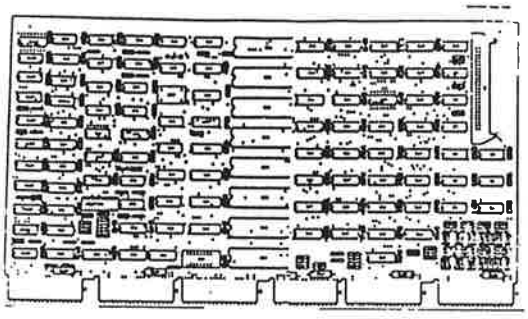
1) LOCATED IN HEX SPC SLOT
2) REQUIRES A DISTRIBUTION PANEL H 317E
3) PRIORITY = BR5
4) DEVICE BASE ADDRESS E81 (1 = ON)
5) " " VECTOR E11 (1 = OFF)
6) DEVICE ADDRESS 160010 - 163776
7) VECTOR ADDRESS 300 - 776

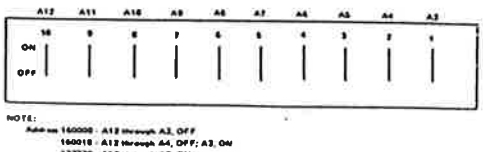
DIAGNOSTIC : ZDZA



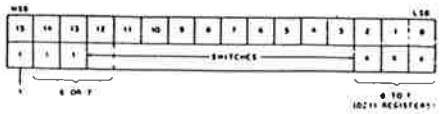
DZ11
8-LINE ASYNCHRONOUS MULTIPLEXER

M7819

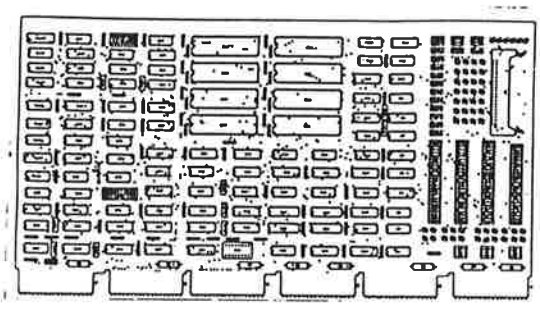


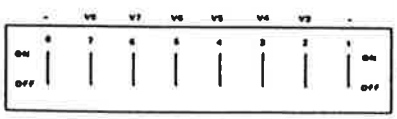


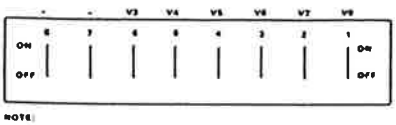
NOTE:
Address 160000 - A12 through A3, OFF
160010 - A12 through A4, OFF; A3, ON
177770 - A12 through A3, ON



M7814







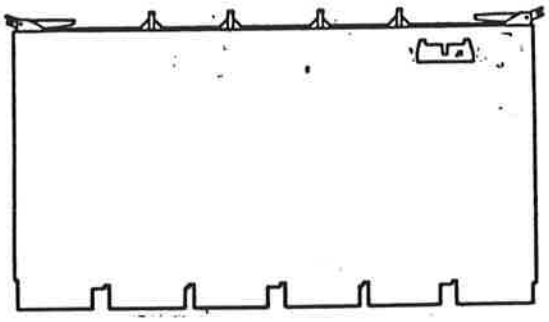
NOTE:
- = OFF
ON = ON

VECTOR	V8	V7	V6	V5	V4	V3
300	ON	-	-	ON	ON	ON
310	ON	-	-	ON	ON	-
	-	-	-	-	-	-
770	-	-	-	-	-	-

HARDWARE AND SOFTWARE COMPATIBLE WITH DEC DZ-11

DIAGNOSTICS ZDZA

CM 7819



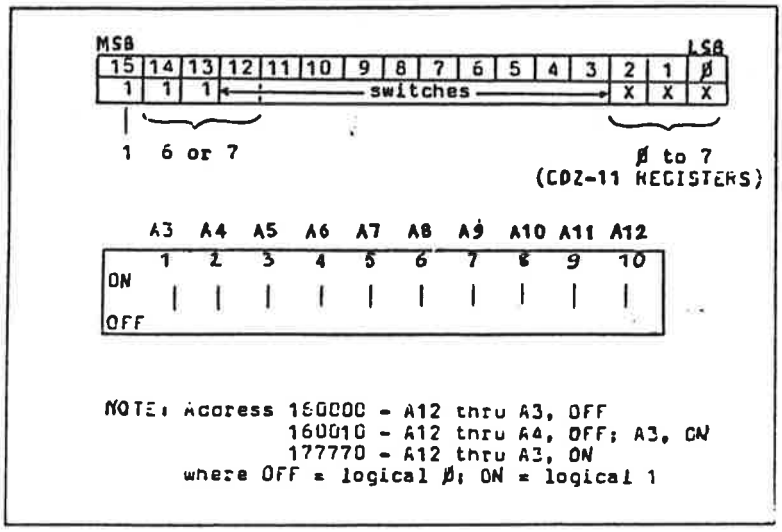


Figure 7. Register Address Selection

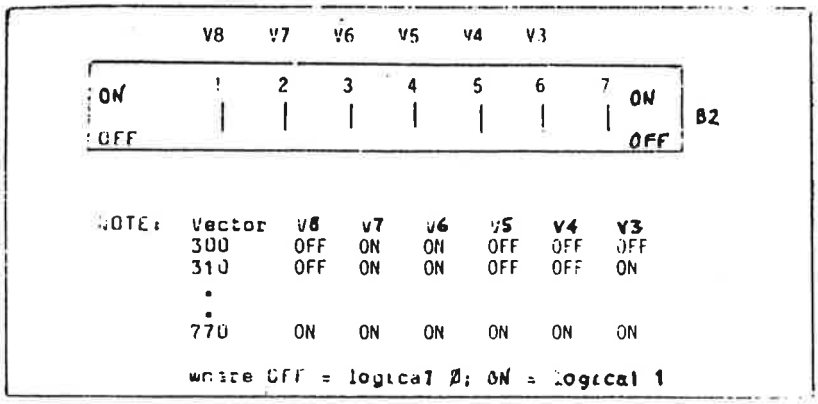


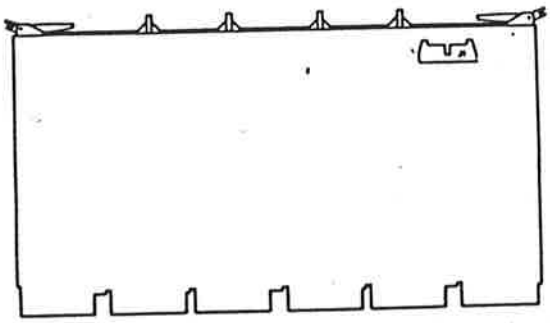
Figure 8. Interrupt Vector Selection

SYSTIME

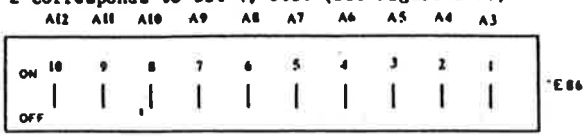
SZ-11

HARDWARE AND SOFTWARE COMPATIBLE WITH DEC DZ-11

DIAGNOSTICS ZDZA



Note that the switch labeled 1 corresponds to bit 3, 2 corresponds to bit 4, etc. (See Figure 2-1.)



NOTE:
Address 160000 - A12 through A3, OFF
160010 - A12 through A4, OFF; A3, ON
177770 - A12 through A3, ON
(OFF = LOGICAL 0, ON = LOGICAL 1)

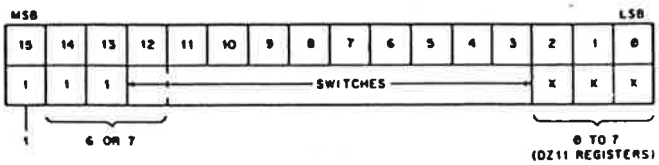
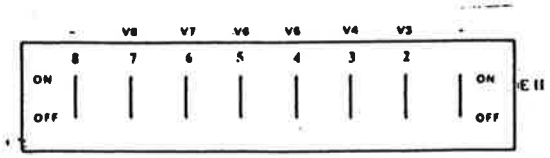


Figure 2-1 SZ11 Address Selection



NOTE
ON = LOGICAL 0
OFF = LOGICAL 1

VECTOR	V8	V7	V6	V5	V4	V3
300	ON	OFF	OFF	ON	ON	ON
310	ON	OFF	OFF	ON	ON	OFF
.						
.						
770	OFF	OFF	OFF	OFF	OFF	OFF

Figure 2-2 SZ11 Vector Selection

DJ11-AC

16-LINE, ASYNCHRONOUS, SERIAL LINE MULTIPLEXER (-AC= 20mA)

(The DH11 does a similar job, but is programmable)
Single system unit, plus distribution panel, which has 16 four-screw terminal strips, for terminal connection.

FIVE DEVICE REGISTERS

76 XXX0 CSR

76 XXX2 Receive buffer reg.

76 XXX4 TX control reg. (CSR bit 10 cleared)

76 XXX4 Break control reg. (CSR bit 10 set)

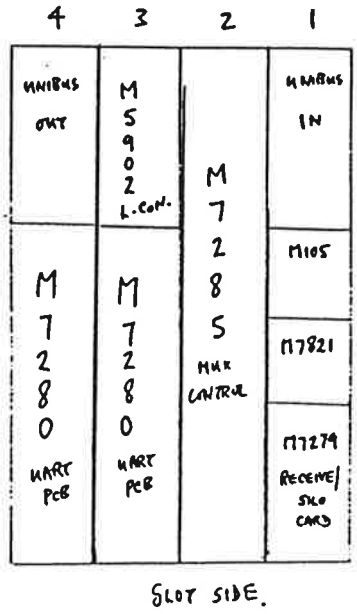
76 XXX6 TX buffer reg.

Addresses, and vectors(2), are in floating address and vector area.

DIAGNOSTICS ZDJA Logic

ZDJB On-line test

DJ 11-AC.

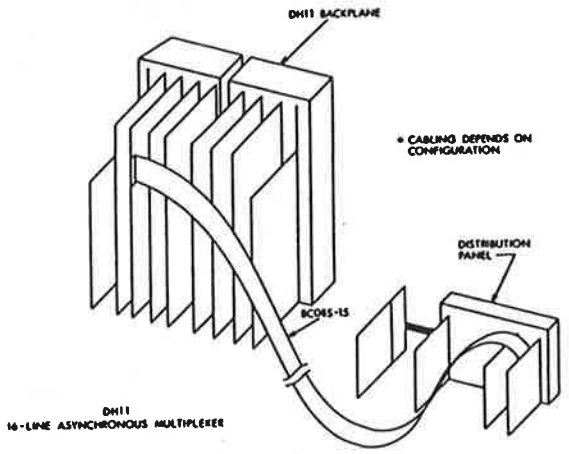


SLOT SIDE.

PLUS H317-A DISTRIBUTION PANEL

PLUS 2× BC08S-15 CABLES.

FEATURES	BENEFITS
Program-selectable speeds up to 9600 bits per second.	Enables the user to attain higher speeds on private or leased lines.
Complete control of each line for: data rate, character size, stop code length, transmission mode.	Offers flexibility to handle wide range of terminal or communication lines.
Program-controlled hardware echo of received characters.	Relieves program of echo function.
64-character hardware buffer for received characters.	Prevents data overrun and subsequent loss of valuable data.
Direct Memory Access for data transfer.	Offers high data throughput and increased flexibility.
Split-speed transmitter and receiver on each line.	More efficient use of communications facilities, and less software demand for receiver.
Hardware break detection and program-controlled break generation.	Enables terminal operator to terminate output or raise attention on half-duplex circuits.



DH11
16-LINE ASYNCHRONOUS MULTIPLEXER

DH11 MODULE UTILISATION

SLOT

	9	8	7	6	5	4	3	2	1
A	M920	M7288	M7360	M7821	M7289	M7277	M7278	M7821	M920
B	Unibus	Line Param CNTL	Prior SEL. *1	INTR CNTL	System CNTL & Recev Scan	Current Addrs & Addrs Select	REG & BYTE Count	NPR CNTL	Unibus
C			M971	M405				M796	
D			Cable Conn. *1	Ext B Clock *2				Unibus Master CNTL	
E	M7279		M7260	M7260				M7247	M7247
F	FIFO Buffer		MULT UART Lines 8–15	MULT UART Lines 0–7				Contl MUX Lines 0–7 *3	Contl MUX Lines 8–15 *4
	M405							M7246	M105
	Ext A Clock *2							CNTL Scan *3	Addrs SEL *4
	M4540								M7821
	DH11 Clock								INTR CNTL *4

VIEWED FROM BOARD SIDE

INTERFACE CABLES

TERMINALS / MODEMS → / INTERFACES ↓	LA34/38	LA35/36	LA120	LA180	VT52/55	VT100 FAMILY	MODEMS DF01-A* (Incl. Cable) DF02-AA/AC DF03-AA/AC
DL11-WA DL11-A,C DLV11-F (20 MA) BC05M	LAX34-CL	N/R	LA12X-AL	(LAXX-NX)	BN52B	VT1XX-AA	–
DL11-WB DL11-B,D DLV11-F (EIA) BC05C	BC22A OR BC03M	(LAXX-KG) BC22A OR BC03M	BC22A OR BC03M	(LAXX-NW) BC22A OR BC03M	BN52A BC22A OR BC03M	BC22A OR BC03M	–
DL11-E DLV11-E (EIA) -BC05C	BC22A OR BC03M	LAXX-KG BC22A OR BC03M	BC22A OR BC03M	LAXX-NW BC22A OR BC03M	BN52A BC22A OR BC03M	BC22A OR BC03M	*USE DF01 CABLE N/R
DLV11-J (20 MA) DLV11-KA	LAX34-CL	N/R	LA12X-AL	LAXX-NX	BN52B	VT1XX-AA	–
DLV11-J (EIA) BC21B	BC22A OR BC03M	LAXX-KG BC22A OR BC03M	BC22A OR BC03M	LAXX-NW BC22A OR BC03M	BN52A BC22A OR BC03M	BC22A OR BC03M	–
DZ11-C,D,F (20 MA) BC04R	LAX34-CL	N/R	LA12X-AL	LAXX-NX	BN52B	VT1XX-AA	–
DZ11-A,B,E (EIA)	BC22A OR BC03M	LAXX-KG BC22A OR BC03M	BC22A OR BC03M	LAXX-NW BC22A OR BC03M	BN52A BC22A OR BC03M	BC22A OR BC03M	*USE DF01 CABLE BC22B BC05D
DZV11-B (EIA) BC11U	BC22A OR BC03M	LAXX-KG BC22A OR BC03M	BC22A OR BC03M	LAXX-NW BC22A OR BC03M	BN52A BC22A OR BC03M	BC22A OR BC03M	N/R *USE DF01 CABLE
MINC SLU0,1,2	BC21C	LAXX-KG BC21C	BC21C	LAXX-NW BC21C	BN52A BC21C	BC21C	–
MODEMS DF01-A* (Incl. Cable) DF02-AA/AC DF03-AA/AC	*N/R BC22B OR BC05D	*N/R LAXX-KG/LG BC22B OR BC05D	*N/R BC22B OR BC05D	*N/R LAXX-NW BC22B OR BC05D	*N/R BN52A BC22B OR BC05D	*N/R BC22B OR BC05D	

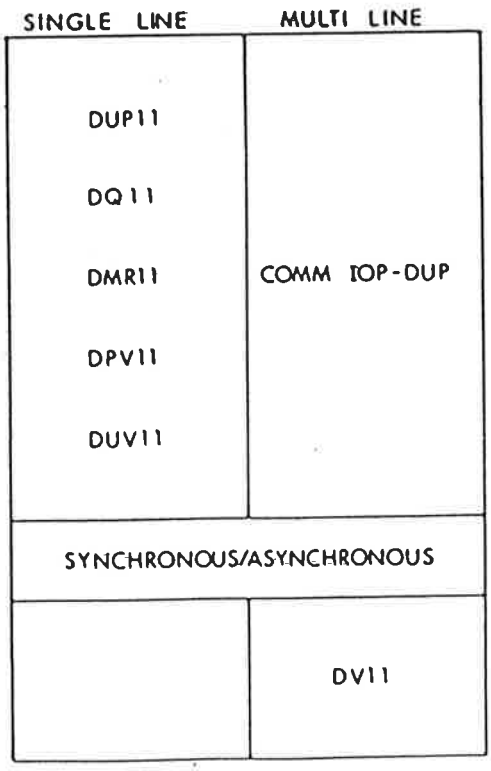
EIA (RS232C) EXTENSION CABLE – BC22B or BC05D

20 MA EXTENSION CABLE – BC05F-XX

VT1XX-AC – BC22A/BC03M

SECTION 4

SYNCHRONOUS COMMUNICATIONS INTERFACES



DU11

Single line program controlled double buffered syn/asyn interface

Modem Control Full/Half Duplex

EIA/Current Mode 201/303 DU11-DA/DU11-EA (DF11-G)

Quad Ht pcb installed in spc slot

Module: M7822

Speed: 10k Baud MAX EIA

100k Baud MAX Current Mode

Cables DU11-DA = BC05C-25

DU11-EA = BC01W-25

Base Address 760010 - (follows DQ11) switch pack 1 (on=0)

Base Vector 300 " " W9-14 (in=1)

Diagnostics: ZDUA-F

DP11 - (DA, DB, DC, CA, KA)

Double Buffered single line synchronous I/O

Synch Character	ASCII	02	Octal
	IBM	32	Hex
	EBCDIC	62	Octal

MODULES		LOCATION
M7075	TX Module	C3
M7065	RX Module	D3
M7223	Control	CDEF 1
M105	Address Selector	C2
M7821	Interrupt Control	D2
G8000	+8V Filter Network	A2

Options:

M405		Clock module	DP11-KA	E2
M239		÷16 Counter	DP11-KA	F2
M594	(DF11-A)	EIA Convertor	(DP11-DA)	D4
M595	(DF11-G)	Current Mode	(DP11-DB/DC)	D4
	DP11-CA	4 Bit Expansion Jumper D4 M7075		
M970		Cable Card Assy		C4

Compatible with 201, 301 and 303 type modems

BASE ADDRESS	774770	M105	Jumper in = Ø
BASE VECTOR	300	M7821	Jumper in = 1

Diagnostics D8DA?

DUP11 - DA

M7867

BC05C-25

BC02-1D

Single line double buffered sychronous I/O full modem control.

Protocols Supported

Byte : DDCMP : BISYNC
Bit : SDLC : HDLC : ADCCP

Error Detection

VRC : LRC

CRC : (DDCMP only)

SPEED 19200 baud with KMC11
9600 baud without KMC11

M7867 installed in SPC slot

W1-7 - Modem control

Base Add E117 160010 SW off = 1

Base Vector E68 300 SW on = 1

Diagnostics

ZDPB
ZDPC
ZDPD
ZDPE

DECX11 Module

DXDPB

DQ11-(DA,EA,AB,BB,KA)

Double buffered, high speed DMA Synchronous interface.

SPEED - UP TO 1 Mega Baud

MODULES		LOCATION
7009467	BACKPLANE DQ11-DA	
M105	ADD DECODER	F1
M7821	INT CONTROLLER	C4
M7815 *	MODEM CONTROL	E1
M7818 *	CHAR DETECT, NPR CONTROL	EF4
M7812 *	BUS SELECTOR	A-F2
M7813 *	CHAR CONTROL, BUS ADD REG	A-F3
OPTIONS		
M7817 *	CHAR DETECTION + SEQ CONTROL (DQ11-BB)	A-F3
M7816 *	A.B. SELECTOR BCC CONTROL (DQ11-AB)	A-F2
M4050 *	XTAL CLOCK DQ11-KA	D4
M594/M970	EIA LEVEL CONVERTER (DQ11-DA)	D1/C1
7009468	BACKPLANE (DQ11-AB-BB)	
M595/M971	CURRENT MODE CONVERTER DQ11-EA	D1/C1

* CHECK SWITCH AND JUMPER OPTIONS Page 2-5

BASE ADD	160010	M105	JUMPER OUT = 1
BASE VECTOR	300	M7821	JUMPER IN = 1
DIAGNOSTICS	ZDQA-B-C-D-E-F-G	Page 3-36	

DV11 COMMUNICATIONS MULTIPLEXER

Synchronous/Asynchronous DMA Device

Microprocessor controlled with 128 character silo buffer

Synchronous Baud Rates 1200, 2400, 4800, 9600
Asynchronous Baud Rates up to 38,400

Modem Control 201, 208, 209
202, 103

Protocols D.D.C.M.P. Bisync

Base Address 775000
Base Vector Follows DUP11 (300)

Modules			Location
	7010834-0-0	Backplane	
	M7807	Bus Control + MUX	C-F1
	M7808	Modem Control, Scan and MUX	C-F9
DV11-AA	M7836	ALU and Bus Transfer	A-F2
	M7837	Unibus Data and NPR Control	A-F3
	M7838	ROM, RAM and Branch Control	A-F4
DV11-BA	M7839x2	Synchronous MUX Line Card	A-F 5 + 6 7 + 8
DV11-BB	M7833x2	Asynchronous " " "	A-F 5 + 6 7 + 8
DV11-BC	M7839x1) M7833x1)	Sync/Async " " "	A-F 5 + 6 7 + 8

KMC-11

AUXILIARY PROCESSOR - REDUCES CPU OVERHEAD AND INCREASES THROUGHPUT

FEATURES

DMA DEVICE
LSI MICROPROCESSOR CONTROLLES
1K x 16 BIT RAM
8 CSR

MODULE
M8204 (REMOVE CA1-CB1 WHEN INSTALLING)
KMC-11 SHOULD BE INSTALLED NEAREST TO PROCESSOR

DIAGNOSTICS

ZKCC
ZKCA
ZKCE

DECX11 MODULE

KMAA

NB TWO BASIC VERSIONS OF DMC-11 (USED IN CONJUNCTION WITH ABOVE)

M8201 - REMOTE MODEM CONTROL
M8202 - COAX - LOCAL NETWORK

SECTION 5

DEC CORE

MM11-L	8K Set of boards (8K Basic Memory Expansion)
MF11-L	24K Backplane for 3 X MM11-L (includes 1st MM11-L)
ME11-L	24K Backplane in a self contained box for 3 X MM11-L (includes 1st MM11-L)

MM11-U	16K Set of boards (16K Basic Mem Expansion)
MF11-U	32K Backplane for 2 X MM11U (includes 1st MM11U)
MM11D	16K Board Modified Unibus
DD11-C or DD11-D	4 slot or 9 slot. Combined Mem/SPC Backplanes.

MOS

MS11-J	16K MOS Modified Backplane

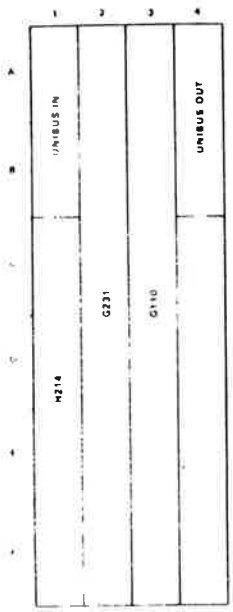
PARITY

Add a 'P' to the memory and backplane designations for the parity versions.

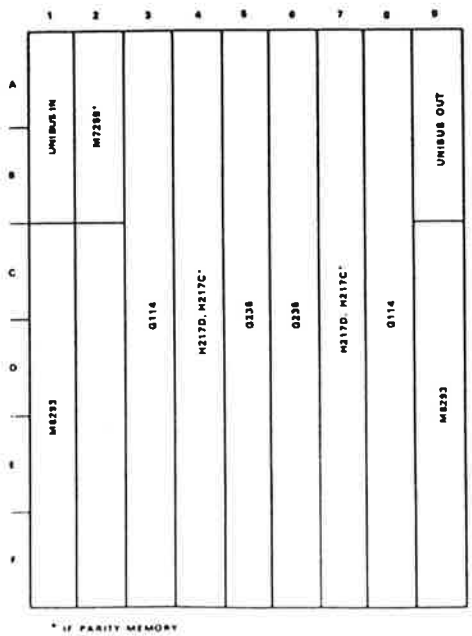
e.g. MM11-U Now equates MM11-UP & fits in an MF11-UP

BACKPLANE	& 1st	EXTENSION	
MF11U	16K X 16	MM11U	2 X SU
MF11UP	16K X 18	MM11UP	2 X SU
	4K X 16	MM11-K	
	8K X 16	MM11-L	
MF11L	12K X 16	MM11-LK	2 X SU
MF11LP	8K X 18	MM11-LP	2 X SU
ME11-L	(8K X 16	MM11-L	5.25" S/C BOX
	(12K X 16	MM11-LK	
MM11-S	8K X 16	MM11-L	1 X SU
MM11F	4K X 16	11/20 CORE	

MM11-S MODULE UTILIZATION

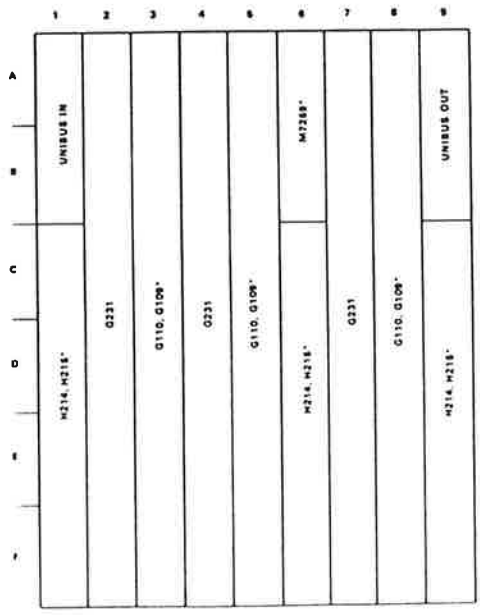


MF11-U(P) MODULE UTILIZATION



* IF PARITY MEMORY

...11-L(P) MODULE UTILIZATION



* IF PARITY MEMORY

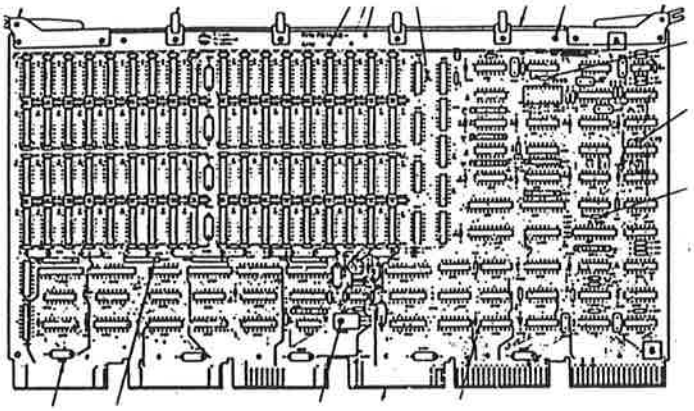
MEMORY

DESCRIPTION	MODULE	BIN	MNEMONIC	LOCATION
16k Core Memory	G652	24888	MM11-DP	A-F 3-8
16k Mos Memory	M7847	37972/24199	MS11-JP	A-F 3-8
Parity Controller	M7850	23219	-	A-B 3-8
64k Mos Memory (Parity)	M7891	31212	MS11-L-B	A-B 3-8
128k Mos Memory (Parity)	M7891	40074	MS11-L-B	A-B 3-8
128k Mos ECC Memory	M8722	37891	MS11-M	1144 EUB
8k CORE MEMORY			MM11-S	Dedicated Backplane
	H214	20670		C-F 1
	G231	4999		A-F 2
	G110	7000		A-F 3
24k CORE MEMORY			MF11-LP	Dedicated Backplane
8k Core Stack	H214/215	20670/30310		CF 1,6 + 9
X,Y Current Source	G231	4999		A-F 2,4 + 7
Sense Inhibit	G110/109	7000/		A-F 3,5 + 8
Parity Module	M7259	21566		A-B 6
32k CORE MEMORY			MF11-UP	Dedicated Backplane
Unibus Timing	M8923	38580		C-F 1 + 9
Parity Module	M7259	21566		A-B 2
8k Core Stack	H217	21569		A-F 4 + 7
X,Y Current Source	G235	21564		A-F 5 + 6
Sense/Inhibit	G114	21563		A-F 3 + 8

NON DEC MEMORY (MOS)

Manufacturer	Size	Model	Bin	Location
Plessy	32kw	PMS1132	36237	SPC
"	63kw	PMS1164	-	"
Systime	32kw	5264	29632	"
"	64kw	5265	32050	"
CDC	64kw	91979	32902	"
"	128kw	94134P	35191	SPC/EUB
Mostek	128kw	MK8015	40233	"
"	64kw	Mk8001	-	SPC
Cambex	128kw	CM1280P	-	SPC/EUB
Cambex Superstore	512kw	SS-11	43909	EUB
Texas Instruments	128kw	TMM20000-01	-	"
" "	256kw	TMM20000-02	-	"
Dataram	64kw	-	-	SPC
National	32kw	NS-11	-	SPC
NISSHO	128kw	1770	-	SPC/EUB

32 KW (64KB) MOS memory (MS11-JP)



STARTING ADDRESS							ENDING ADDRESS						
OCTAL	DECIMAL BYTES	SW1-1	SW1-2	SW1-3	SW1-4	SW1-5	OCTAL	DECIMAL BYTES	SW1-6	SW1-7	SW1-8	SW1-9	SW1-10
000000	0K	ON	ON	ON	ON	ON	017776	8K	OFF	ON	ON	ON	ON
020000	8K	OFF	ON	ON	ON	ON	037776	16K	ON	OFF	ON	ON	ON
040000	16K	ON	OFF	ON	ON	ON	057776	24K	OFF	OFF	ON	ON	ON
060000	24K	OFF	OFF	ON	ON	ON	077776	32K	ON	ON	OFF	ON	ON
100000	32K	ON	ON	OFF	ON	ON	117776	40K	OFF	ON	OFF	ON	ON
120000	40K	OFF	ON	OFF	ON	ON	137776	48K	ON	OFF	OFF	ON	ON
140000	48K	ON	OFF	OFF	ON	ON	157776	56K	OFF	OFF	OFF	ON	ON
160000	56K	OFF	OFF	OFF	ON	ON	177776	64K	ON	ON	ON	OFF	ON
200000	64K	ON	ON	ON	OFF	ON	217776	72K	OFF	ON	ON	OFF	ON
220000	72K	OFF	ON	ON	OFF	ON	237776	80K	ON	OFF	ON	OFF	ON
240000	80K	ON	OFF	ON	OFF	ON	257776	88K	OFF	OFF	ON	OFF	ON
260000	88K	OFF	OFF	ON	OFF	ON	277776	96K	ON	ON	OFF	OFF	ON
300000	96K	ON	ON	OFF	OFF	ON	317776	104K	OFF	ON	OFF	OFF	ON
320000	104K	OFF	ON	OFF	OFF	ON	337776	112K	ON	OFF	OFF	OFF	ON
340000	112K	ON	OFF	OFF	OFF	ON	357776	120K	OFF	OFF	OFF	OFF	ON
360000	120K	OFF	OFF	OFF	OFF	ON	377776	128K	ON	ON	ON	ON	OFF
400000	128K	ON	ON	ON	ON	OFF	417776	136K	OFF	ON	ON	ON	OFF
420000	136K	OFF	ON	ON	ON	OFF	437776	144K	ON	OFF	ON	ON	OFF
440000	144K	ON	OFF	ON	ON	OFF	457776	152K	OFF	OFF	ON	ON	OFF
460000	152K	OFF	OFF	ON	ON	OFF	477776	160K	ON	ON	OFF	ON	OFF
500000	160K	ON	ON	OFF	ON	OFF	517776	168K	OFF	ON	OFF	ON	OFF
520000	168K	OFF	ON	OFF	ON	OFF	537776	176K	ON	OFF	OFF	ON	OFF
540000	176K	ON	OFF	OFF	ON	OFF	557776	184K	OFF	OFF	OFF	ON	OFF
560000	184K	OFF	OFF	OFF	ON	OFF	577776	192K	ON	ON	ON	OFF	OFF
600000	192K	ON	ON	ON	OFF	OFF	617776	200K	OFF	ON	ON	OFF	OFF
620000	200K	OFF	ON	ON	OFF	OFF	637776	208K	ON	OFF	ON	OFF	OFF
640000	208K	ON	OFF	ON	OFF	OFF	657776	216K	OFF	OFF	ON	OFF	OFF
660000	216K	OFF	OFF	ON	OFF	OFF	677776	224K	ON	ON	OFF	OFF	OFF
700000	224K	ON	ON	OFF	OFF	OFF	717776	232K	OFF	ON	OFF	OFF	OFF
720000	232K	OFF	ON	OFF	OFF	OFF	737776	240K	ON	OFF	OFF	OFF	OFF
740000	240K	ON	OFF	OFF	OFF	OFF	757776	248K	OFF	OFF	OFF	OFF	OFF

NOTE: To disable the memory from being selected, switches position SW1-1 to SW1-5 and SW1-6 to SW1-10 should be the same.

TABLE 2-4: PM-S11 32 ADDRESS SWITCH SETTINGS

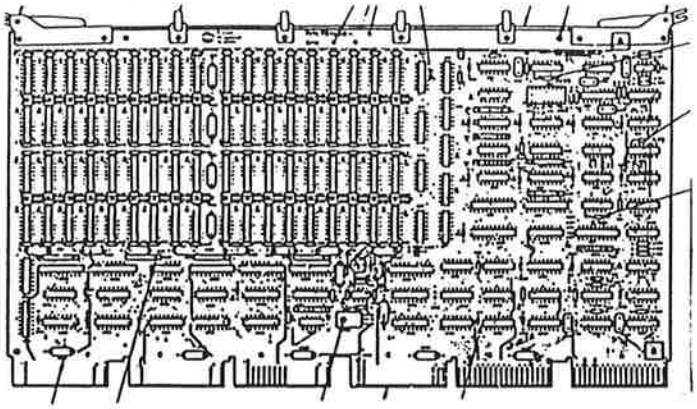
CAPACITY	CONFIGURATION	PART NUMBER	MODEL NUMBER
8K byte	Parity	700755-107	PM-S1132/107
8K bytes	Parity	700755-115	PM-S1132/115
16K bytes	Parity	700755-106	PM-S1132/106
16K bytes	Parity	700755-114	PM-S1132/114
24K bytes	Parity	700755-105	PM-S1132/105
24K bytes	Parity	700755-113	PM-S1132/113
32K bytes	Parity	700755-104	PM-S1132/104
32K bytes	Parity	700755-112	PM-S1132/112
40K bytes	Parity	700755-103	PM-S1132/103
40K bytes	Parity	700755-111	PM-S1132/111
48K bytes	Parity	700755-102	PM-S1132/102
48K bytes	Parity	700755-110	PM-S1132/110
56K bytes	Parity	700755-101	PM-S1132/101
56K bytes	Parity	700755-109	PM-S1132/109
64K bytes	Parity	700755-100	PM-S1132/100
64K bytes	Parity	700755-108	PM-S1132/108
8K bytes	Non-Parity	700755-207	PM-S1132/207
16K bytes	Non-Parity	700755-206	PM-S1132/206
24K bytes	Non-Parity	700755-205	PM-S1132/205
32K bytes	Non-Parity	700755-204	PM-S1132/204
40K bytes	Non-Parity	700755-203	PM-S1132/203
48K bytes	Non-Parity	700755-202	PM-S1132/202
56K bytes	Non-Parity	700755-201	PM-S1132/201
64K bytes	Non-Parity	700755-200	PM-S1132/200

FUNCTION	JUMPER CONNECTIONS
Modified Unibus (100 series)	
Battery Option	W1-W3, W4-W6, W7-W8, W9-W10, W12-W14
No Battery Option	W1-W3, W4-W6, W7-W8, W9-W11, W12-W13
Standard Unibus (200 series)	W9-W11, W12-W13
30K Option	1. Cut etch between U169-1 and U169-2 (solder side) 2. Jumper W15 and W16 3. Lift pins U166-5 and U166-15 4. Jumper U166-6 to U166-14 to U166-7 (ground)
31K Option	1. Cut etch between U169-1 and U169-2 (solder side) 2. Jumper W15 and W16 3. Cut etch between U188-5 and U188-6 (solder sides) 4. Jumper W26 to U188-6 (verify that W25 is not jumpered to W26) 5. Lift pins U166-5 and U166-15 6. Jumper U166-6 to U166-14 to U166-7 (ground)

*The battery option is not available for the standard Unibus.

Table 2-2: Jumper Connections for Memory Configurations

64KW (128KB) MOS memory with parity controller (MS11-L)



STARTING ADDRESS							ENDING ADDRESS						
OCTAL	DECIMAL BYTES	SW1-1	SW1-2	SW1-3	SW1-4	SW1-5	OCTAL	DECIMAL BYTES	SW1-6	SW1-7	SW1-8	SW1-9	SW1-10
000000	0K	ON	ON	ON	ON	ON	017776	8K	OFF	ON	ON	ON	ON
020000	8K	OFF	ON	ON	ON	ON	037776	16K	ON	OFF	ON	ON	ON
040000	16K	ON	OFF	ON	ON	ON	057776	24K	OFF	OFF	ON	ON	ON
060000	24K	OFF	OFF	ON	ON	ON	077776	32K	ON	ON	OFF	ON	ON
100000	32K	ON	ON	OFF	ON	ON	117776	40K	OFF	ON	OFF	ON	ON
120000	40K	OFF	ON	OFF	ON	ON	137776	48K	ON	OFF	OFF	ON	ON
140000	48K	ON	OFF	OFF	ON	ON	157776	56K	OFF	OFF	OFF	ON	ON
160000	56K	OFF	OFF	OFF	ON	ON	177776	64K	ON	ON	ON	OFF	ON
200000	64K	ON	ON	ON	OFF	ON	217776	72K	OFF	ON	ON	OFF	ON
220000	72K	OFF	ON	ON	OFF	ON	237776	80K	ON	OFF	ON	OFF	ON
240000	80K	ON	OFF	ON	OFF	ON	257776	88K	OFF	OFF	ON	OFF	ON
260000	88K	OFF	OFF	ON	OFF	ON	277776	96K	ON	ON	OFF	OFF	ON
300000	96K	ON	ON	OFF	OFF	ON	317776	104K	OFF	ON	OFF	OFF	ON
320000	104K	OFF	ON	OFF	OFF	ON	337776	112K	ON	OFF	OFF	OFF	ON
340000	112K	ON	OFF	OFF	OFF	ON	357776	120K	OFF	OFF	OFF	OFF	ON
360000	120K	OFF	OFF	OFF	OFF	ON	377776	128K	ON	ON	ON	ON	OFF
400000	128K	ON	ON	ON	ON	OFF	417776	136K	OFF	ON	ON	ON	OFF
420000	136K	OFF	ON	ON	ON	OFF	437776	144K	ON	OFF	ON	ON	OFF
440000	144K	ON	OFF	ON	ON	OFF	457776	152K	OFF	OFF	ON	ON	OFF
460000	152K	OFF	OFF	ON	ON	OFF	477776	160K	ON	ON	OFF	ON	OFF
500000	160K	ON	ON	OFF	ON	OFF	517776	168K	OFF	ON	OFF	ON	OFF
520000	168K	OFF	ON	OFF	ON	OFF	537776	176K	ON	OFF	OFF	ON	OFF
540000	176K	ON	OFF	OFF	ON	OFF	557776	184K	OFF	OFF	OFF	ON	OFF
560000	184K	OFF	OFF	OFF	ON	OFF	577776	192K	ON	ON	ON	OFF	OFF
600000	192K	ON	ON	ON	OFF	OFF	617776	200K	OFF	ON	ON	OFF	OFF
620000	200K	OFF	ON	ON	OFF	OFF	637776	208K	ON	OFF	ON	OFF	OFF
640000	208K	ON	OFF	ON	OFF	OFF	657776	216K	OFF	OFF	ON	OFF	OFF
660000	216K	OFF	OFF	ON	OFF	OFF	677776	224K	ON	ON	OFF	OFF	OFF
700000	224K	ON	ON	OFF	OFF	OFF	717776	232K	OFF	ON	OFF	OFF	OFF
720000	232K	OFF	ON	OFF	OFF	OFF	737776	240K	ON	OFF	OFF	OFF	OFF
740000	240K	ON	OFF	OFF	OFF	OFF	757776	248K	OFF	OFF	OFF	OFF	OFF

NOTE: To disable the memory from being selected, switches position SW1-1 to SW1-5 and SW1-6 to SW1-10 should be the same.

TABLE 2-4: PM-S1164A ADDRESS SWITCH SETTINGS

IF THE PARITY CONTROLLER IS THE:	SET CSR ADDRESS TO:	SW2 POSITION			
		1	2	3	4
1st	772100	ON	ON	ON	ON
→ 2nd	772102	OFF	ON	ON	ON
3rd	772104	ON	OFF	ON	ON
4th	772106	OFF	OFF	ON	ON
5th	772110	ON	ON	OFF	ON
6th	772112	OFF	ON	OFF	ON
7th	772114	ON	OFF	OFF	ON
8th	772116	OFF	OFF	OFF	ON
9th	772120	ON	ON	ON	OFF
10th	772122	OFF	ON	ON	OFF
11th	772124	ON	OFF	ON	OFF
12th	772126	OFF	OFF	ON	OFF
13th	772130	ON	ON	OFF	OFF
14th	772132	OFF	ON	OFF	OFF
15th	772134	ON	OFF	OFF	OFF
16th	772136	OFF	OFF	OFF	OFF

TABLE 2-5: PARITY CONTROLLER, CSR ADDRESS SELECT

8-64 KW parity memory

MK8001 INSTALLATION OPTIONS–BOARD STRAPPING
Table 2-3

FOR MODIFIED UNIBUS

E18-E19
E41-E42

E49-E50 for core power supply
E51-E52 for semi power supply.

E63-E64 w/o battery back-up or
E67-E68 with battery back-up.

E43-E44 with parity
E46-E47 with parity

FOR STANDARD UNIBUS

E53-E54
E63-E64

E44-E45 with parity and or
E47-E48 with parity.

TERMINATORS (For Last Slot of Unibus)

E8-E9
E40-E41
E55-E56
E57-E58
E59-E60
E61-E62

Jumpers other than the above are manufacturing options only. Do not change.

ADDRESS DIP SWITCH SETTING
Table 2-4

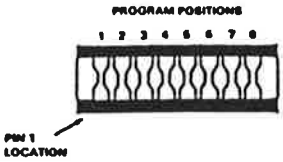
START ADDRESS	S5	S4	S3	S2	S1
0	0	0	0	0	0
4K	0	0	0	0	1
8K	0	0	0	1	0
12K	0	0	0	1	1
16K	0	0	1	0	0
20K	0	0	1	0	1
24K	0	0	1	1	0
28K	0	0	1	1	1
32K	0	1	0	0	0
36K	0	1	0	0	1
40K	0	1	0	1	0
44K	0	1	0	1	1
48K	0	1	1	0	0
52K	0	1	1	0	1
56K	0	1	1	1	0
60K	0	1	1	1	1
64K	1	0	0	0	0
68K	1	0	0	0	1
72K	1	0	0	1	0
76K	1	0	0	1	1
80K	1	0	1	0	0
84K	1	0	1	0	1
88K	1	0	1	1	0
92K	1	0	1	1	1
96K	1	1	0	0	0
100K	1	1	0	0	1
104K	1	1	0	1	0
108K	1	1	0	1	1
112K	1	1	1	0	0
116K	1	1	1	0	1
120K	1	1	1	1	0
124K	1	1	1	1	1

I/O Page Size	S6	S7	S8
4K	0	0	Close for 32K machine using I/O page 4K
NA	1	0	
2K	0	1	
1K	1	1	

"0" = OPEN

"1" = CLOSED

PROGRAMMABLE HEADER



INSTALLATION OPTIONS - BOARD STRAPPING

POWER CONFIGURATIONS		JUMPERS					
Code	Application	E1-E2	CU1 E3-E4	CA2 E6-E6	BD1 E7-E8	AV2 E9-E10	AR1 E11-E12
A	Modified Unibus - Semiconductor (+15 V) Supply W/O Batt	Out	Out	In	Out	Out	In
B	Modified Unibus - Semiconductor (+15 V) Supply W/Batt	Out	Out	Out	In	Out	In
C	Modified Unibus - Semiconductor (+12 V) Supply W/O Batt	In	Out	In	Out	Out	In
D	Modified Unibus - Semiconductor (+12 V) Supply W/Batt	In	Out	Out	In	Out	In
E	Modified Unibus - Core (+20 V) Supply	Out	Out	In	Out	In	Out
F	Standard Unibus (+15 V) Supply	Out	In	In	Out	Out	Out

ARRAY CONFIGURATIONS, HEADER LOCATION U13K

ROWS ENABLED* \ PROGRAM POSITION	1	2	3	4	5	6	7	8
A, K	OUT	OUT	OUT	OUT	OUT	OUT	OUT	N/A
A, B, K, L	IN	OUT	OUT	OUT	OUT	OUT	OUT	N/A
A, B, C, K, L, M	IN	IN	OUT	OUT	OUT	OUT	OUT	N/A
A, B, C, D, K, L, M, N	IN	IN	IN	OUT	OUT	OUT	OUT	N/A
A, B, C, D, E, K, L, M, N, P	IN	IN	IN	IN	OUT	OUT	OUT	N/A
A, B, C, D, E, F, K, L, M, N, P, R	IN	IN	IN	IN	IN	OUT	OUT	N/A
A, B, C, D, E, F, H, K, L, M, N, P, R, S	IN	IN	IN	IN	IN	IN	OUT	N/A
A, B, C, D, E, F, H, J, K, L, M, N, P, R, S, T	IN	IN	IN	IN	IN	IN	IN	N/A

*Note - Rows A-J are the upper byte and rows K-T are the lower byte of the 16 bit data word. Rows are organized relative to address significance (i.e. Rows A & K represent the first 8K or 16K words).

PARITY ENABLE, HEADER LOCATION U14V

PROGRAM POSITION	1	2	3	4	5	6	7	8
Parity Enabled	*	*	*	OUT	OUT	*	*	*
Parity Disabled	*	*	*	IN	IN	*	*	*

*Manufacturing use only

STARTING ADDRESS SWITCH SETTINGS

STARTING ADDRESS STANDARD MODE		EXT Mode Switch	SWITCH SETTING 0 OFF 1 ON							
DEC (K words)	OCTAL	S17N-7	S21L-8	S21L-7	S21L-6	S21L-5	S21L-4	S21L-3	S21L-2	S21L-1
0	000000	0	0	0	0	0	0	0	0	0
8	040000	0	0	0	0	0	0	0	0	1
16	100000	0	0	0	0	0	0	0	1	0
24	140000	0	0	0	0	0	0	0	1	1
32	200000	0	0	0	0	0	0	1	0	0
40	240000	0	0	0	0	0	0	1	0	1
48	300000	0	0	0	0	0	0	1	1	0
56	340000	0	0	0	0	0	0	1	1	1
64	400000	0	0	0	0	0	1	0	0	0
72	440000	0	0	0	0	0	1	0	0	1
80	500000	0	0	0	0	0	1	0	1	0
88	540000	0	0	0	0	0	1	0	1	1
96	600000	0	0	0	0	0	1	1	0	0
104	640000	0	0	0	0	0	1	1	0	1
112	700000	0	0	0	0	0	1	1	1	0
120	740000	0	0	0	0	0	1	1	1	1
STARTING ADDRESS RANGE EXTENDED MODE = 11/44										
0 - 120	000000000 - 007400000	1	0	0	0	0				
128 - 248	010000000 - 017400000	1	0	0	0	1				
256 - 376	020000000 - 027400000	1	0	0	1	0				
384 - 504	030000000 - 037400000	1	0	0	1	1				
512 - 632	040000000 - 047400000	1	0	1	0	0				
640 - 760	050000000 - 057400000	1	0	1	0	1				
768 - 888	060000000 - 067400000	1	0	1	1	0				
896 - 1016	070000000 - 077400000	1	0	1	1	1				
1024 - 1144	100000000 - 107400000	1	1	0	0	0				
1152 - 1272	110000000 - 117400000	1	1	0	0	1				
1280 - 1400	120000000 - 127400000	1	1	0	1	0				
1408 - 1528	130000000 - 137400000	1	1	0	1	1				

TO OBTAIN 8K BOUNDARY SETTINGS WITHIN THE SPECIFIED RANGE, REPEAT SWITCH SETTINGS FROM THE ABOVE 0-128K TABLE
I.E. 520K = S.A.
S17N - 7 = 1 ON
S21L - 7 = 1 = ON
S21L - 2 = 1 ON

(Continued)

STARTING ADDRESS EXTENDED MODE		EXT Mode Switch	SWITCH SETTING 0 OFF 1 ON			
1536 - 1656	140000000 - 147400000	1	1	1	0	0
1664 - 1784	150000000 - 157400000	1	1	1	0	1
1792 - 1912	160000000 - 167400000	1	1	1	1	0
1920 - 2040	170000000 - 177400000	1	1	1	1	1

PARITY REGISTER ADDRESS SWITCH SETTINGS

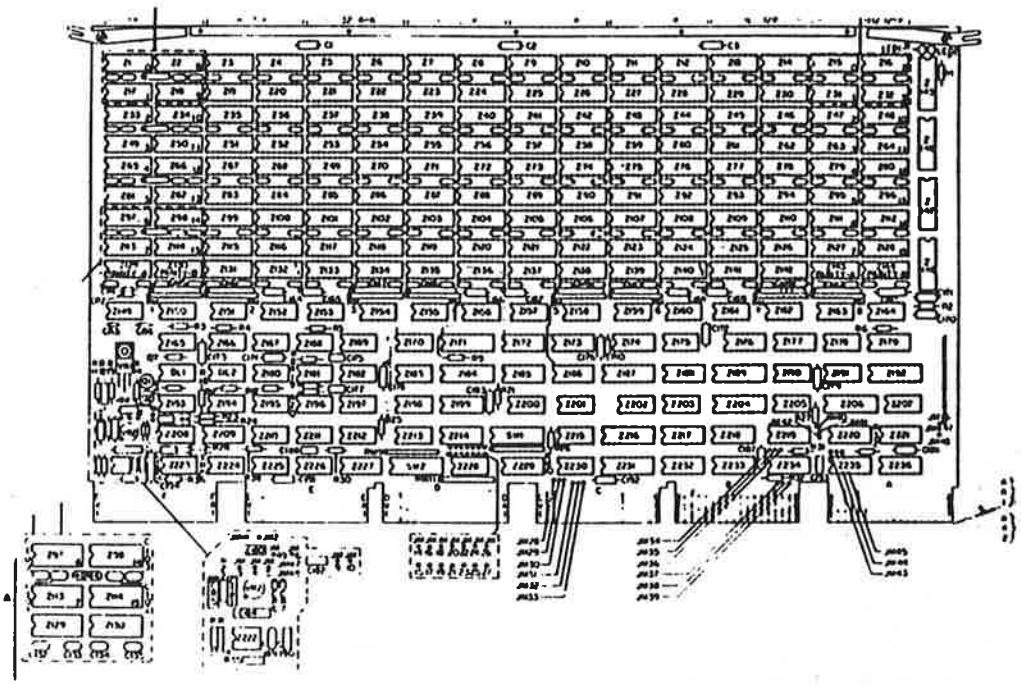
PARITY REGISTER ADDRESS (OCTAL)		SWITCH SETTINGS 0-OFF 1-ON			
EXTENDED S17N - 7 = 1 = ON	STANDARD S17N - 7 = 0 = OFF	S17N-4	S17N-3	S17N-2	S
17772100 = 11/44	772100	1	1	1	
17772102	772102	1	1	1	0
17772104	772104	1	1	0	1
17772106	772106	1	1	0	0
17772110	772110	1	0	1	1
17772112	772112	1	0	1	0
17772114	772114	1	0	0	1
17772116	772116	1	0	0	0
17772120	772120	0	1	1	1
17772122	772122	0	1	1	0
17772124	772124	0	1	0	1
17772126	772126	0	1	0	0
17772130	772130	0	0	1	1
17772132	772132	0	0	1	0
17772134	772134	0	0	0	1
17772136	772136	0	0	0	0

PAGE SWITCH SETTINGS

0 - OFF 1 - ON

MEMORY SIZE	I/O PAGE SIZE	S17N-6	S17N-5	S21E-4
128K	2K (Not for use in 32K Machines)	1	1	1
124K	4K (Standard Size)	1	0	1
120K	8K (Extended Size)	0	0	1
110K	16K (Special Size - 112K Boards Only)	1	1	0
108K	20K (Special Size - 112K Boards Only)	1	0	0
104K	24K (Special Size - 112K Boards Only)	0	0	0

128KW parity memory (MS11-L)



15 FOR EXTERNAL VDD MARGIN, INSTALL JM4 TO JM49
FOR INTERNAL VDD MARGIN, CONNECT TEST FIXTURE TO JM3, JM4 & JM5

16 TO DISABLE REFRESH, STRAP JM9 TO JM10

17 EXTENDED ADDRESS BUS, STRAP JM37 TO JM39, JM41 TO JM43 JM42 TO JM43 & JM34 TO JM35

PARITY CONTROL FOR EXTERNAL MEMORY STRAP JM37 TO JM38, JM44 TO JM45, JM40 TO JM42 & JM36 TO JM35

18 STRAP JM28 TO JM29 FOR 16K RAMS, STRAP JM29 TO JM30 FOR 32K RAM USE

14 STARTING ADDRESS SELECT TABLE

PART 1

PARTIAL STARTING ADDRESS		SWITCH POSITIONS				
DECIMAL	OCTAL	SW2-5 (A17)	SW2-4 (A16)	SW2-3 (A15)	SW2-2 (A14)	SW2-1 (A13)
0 K	SS000000	OFF	OFF	OFF	OFF	OFF
4 K	SS020000	OFF	OFF	OFF	OFF	ON
8 K	SS040000	OFF	OFF	OFF	ON	OFF
12 K	SS060000	OFF	OFF	OFF	ON	ON
16 K	SS100000	OFF	OFF	ON	OFF	OFF
20 K	SS120000	OFF	OFF	ON	OFF	ON
24 K	SS140000	OFF	OFF	ON	ON	OFF
28 K	SS160000	OFF	OFF	ON	ON	ON
32 K	SS200000	OFF	ON	OFF	OFF	OFF
36 K	SS220000	OFF	ON	OFF	OFF	ON
40 K	SS240000	OFF	ON	OFF	ON	OFF
44 K	SS260000	OFF	ON	OFF	ON	ON
48 K	SS300000	OFF	ON	ON	OFF	OFF
52 K	SS320000	OFF	ON	ON	OFF	ON
56 K	SS340000	OFF	ON	ON	ON	OFF
60 K	SS360000	OFF	ON	ON	ON	ON
64 K	SS400000	ON	OFF	OFF	OFF	OFF
68 K	SS420000	ON	OFF	OFF	OFF	ON
72 K	SS440000	ON	OFF	OFF	ON	OFF
76 K	SS460000	ON	OFF	OFF	ON	ON
80 K	SS500000	ON	OFF	ON	OFF	OFF
84 K	SS520000	ON	OFF	ON	OFF	ON
88 K	SS540000	ON	OFF	ON	ON	OFF
92 K	SS560000	ON	OFF	ON	ON	ON
96 K	SS600000	ON	ON	OFF	OFF	OFF
100 K	SS620000	ON	ON	OFF	OFF	ON
104 K	SS640000	ON	ON	OFF	ON	OFF
108 K	SS660000	ON	ON	OFF	ON	ON
112 K	SS700000	ON	ON	ON	OFF	OFF
116 K	SS720000	ON	ON	ON	OFF	ON
120 K	SS740000	ON	ON	ON	ON	OFF
124 K	SS760000	ON	ON	ON	ON	ON

NOTE: SS = OCTAL DIGITS DETERMINED BY SWITCHES SW2-6 TO SW2-9.
RR = OCTAL DIGITS DETERMINED BY SWITCHES SW2-1 TO SW2-5

PART 2

PARTIAL STARTING ADDRESS		SWITCH POSITIONS			
DECIMAL	OCTAL	SW2-9 (A21)	SW2-8 (A20)	SW2-7 (A19)	SW2-6 (A18)
0 K	00RR0000	OFF	OFF	OFF	OFF
128 K	01RR0000	OFF	OFF	OFF	ON
256 K	02RR0000	OFF	OFF	ON	OFF
384 K	03RR0000	OFF	OFF	ON	ON
512 K	04RR0000	OFF	ON	OFF	OFF
640 K	05RR0000	OFF	ON	OFF	ON
768 K	06RR0000	OFF	ON	ON	OFF
896 K	07RR0000	OFF	ON	ON	ON
1024 K	10RR0000	ON	OFF	OFF	OFF
1152 K	11RR0000	ON	OFF	OFF	ON
1280 K	12RR0000	ON	OFF	ON	OFF
1408 K	13RR0000	ON	OFF	ON	ON
1536 K	14RR0000	ON	ON	OFF	OFF
1664 K	15RR0000	ON	ON	OFF	ON
1792 K	16RR0000	ON	ON	ON	OFF
1920 K	17RR0000	ON	ON	ON	ON

13 CSR ADDRESS SELECTION

UNIBUS ADDRESS	EXTENDED BUS ADDRESS	SWITCH POSITIONS				
		SW1-5 (DISABLE)	SW1-4 (A04)	SW1-3 (A03)	SW1-2 (A02)	SW1-1 (A01)
772100	17772100	OFF	ON	ON	ON	ON
772102	17772102	OFF	ON	ON	ON	OFF
772104	17772104	OFF	ON	ON	OFF	ON
772106	17772106	OFF	ON	ON	OFF	OFF
772110	17772110	OFF	ON	OFF	ON	ON
772112	17772112	OFF	ON	OFF	ON	OFF
772114	17772114	OFF	ON	OFF	OFF	ON
772116	17772116	OFF	ON	OFF	OFF	OFF
772120	17772120	OFF	OFF	ON	ON	ON
772122	17772122	OFF	OFF	ON	ON	OFF
772124	17772124	OFF	OFF	ON	OFF	ON
772126	17772126	OFF	OFF	ON	OFF	OFF
772130	17772130	OFF	OFF	OFF	ON	ON
772132	17772132	OFF	OFF	OFF	ON	OFF
772134	17772134	OFF	OFF	OFF	OFF	ON
772136	17772136	OFF	OFF	OFF	OFF	OFF
DISABLE	DISABLE	ON	X	X	X	X

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RESERVE I/O SPACE

PERIPHERAL PAGE SIZE	UNIBUS LOCATION	EXTENDED BUS LOCATION	SWITCH POSITIONS SW1-9 EXTENDED MEMORY BUS	SW1-8 MGT ADR	SW1-7 (A12)	SW1-6 (A13)
2K	126K-128K	N/A	OFF	ON	ON	ON
4K	124K-128K	N/A	OFF	ON	OFF	ON
8K	120K-128K	N/A	OFF	ON	OFF	OFF
2K	N/A	2046K-2048K	ON	ON	ON	ON
4K	N/A	2044K-2048K	ON	ON	OFF	ON
8K	N/A	2040K-2048K	ON	ON	OFF	OFF

TO DISABLE I/O SPACE SW2-10 ON

9 VERSION CHART

SIZE	UNIBUS	VOLTAGE	PARITY	JUMPER
128KX18	STANDARD	+15V	YES	JM31 TO JM32
128KX18	MODIFIED	+5V +12V	YES	JM31 TO JM33

128W memory

DIAGNOSTICS:

ZQMC
ZMSD

SuperSTOR-11 Memory Configurations

Model Designation	Word Bit Length	Data Word Capacity
CM1600	16	16K
CM1600P	18	16K
CM3200	16	32K
CM3200P	18	32K
CM4800	16	48K
CM4800P	18	48K
CM6400	16	64K
CM6400P	18	64K
CM8000	16	80K
CM8000P	18	80K
CM9600	16	96K
CM9600P	18	96K
CM1120	16	112K
CM1120P	18	112K
CM1280	16	128K
CM1280P	18	128K

Starting Address	S1-1	S1-2	S1-3	S1-4	S1-5
0K	0	0	0	0	0
4K	0	0	0	0	1
8K	0	0	0	1	0
12K	0	0	0	1	1
16K	0	0	1	0	0
20K	0	0	1	0	1
24K	0	0	1	1	0
28K	0	0	1	1	1
32K	0	1	0	0	0
36K	0	1	0	0	1
40K	0	1	0	1	0
44K	0	1	0	1	1
48K	0	1	1	0	0
52K	0	1	1	0	1
56K	0	1	1	1	0
60K	0	1	1	1	1
64K	1	0	0	0	0
68K	1	0	0	0	1
72K	1	0	0	1	0
76K	1	0	0	1	1
80K	1	0	1	0	0
84K	1	0	1	0	1
88K	1	0	1	1	0
92K	1	0	1	1	1
96K	1	1	0	0	0
100K	1	1	0	0	1
104K	1	1	0	1	0
108K	1	1	0	1	1
112K	1	1	1	0	0
116K	1	1	1	0	1
120K	1	1	1	1	0
124K	1	1	1	1	1

0 = OFF Position 1 = ON Position

Ending Address	S1-6	S1-7	S1-8	S2-5	S2-6
0K	0	0	0	0	0
4K	0	0	0	0	1
8K	0	0	0	1	0
12K	0	0	0	1	1
16K	0	0	1	0	0
20K	0	0	1	0	1
24K	0	0	1	1	0
28K	0	0	1	1	1
32K	0	1	0	0	0
36K	0	1	0	0	1
40K	0	1	0	1	0
44K	0	1	0	1	1
48K	0	1	1	0	0
52K	0	1	1	0	1
56K	0	1	1	1	0
60K	0	1	1	1	1
64K	1	0	0	0	0
68K	1	0	0	0	1
72K	1	0	0	1	0
76K	1	0	0	1	1
80K	1	0	1	0	0
84K	1	0	1	0	1
88K	1	0	1	1	0
92K	1	0	1	1	1
96K	1	1	0	0	0
100K	1	1	0	0	1
104K	1	1	0	1	0
108K	1	1	0	1	1
112K	1	1	1	0	0
116K	1	1	1	0	1
120K	1	1	1	1	0
124K	1	1	1	1	1

JUMPER FUNCTION SUMMARY LIST

CSR Address	S2-1	S2-2	S2-3	S2-4
772100	1	1	1	1
772102	1	1	1	0
772104	1	1	0	1
772106	1	1	0	0
772110	1	0	1	1
772112	1	0	1	0
772114	1	0	0	1
772116	1	0	0	0
772120	0	1	1	1
772122	0	1	1	0
772124	0	1	0	1
772126	0	1	0	0
772130	0	0	1	1
772132	0	0	1	0
772134	0	0	0	1
772136	0	0	0	0

0 = OFF Position 1 = ON Position

J1, J2	Power Option +5v or +5 BBU
J3, J4	Power Option +12v or +15v
E1 thru E36	Delay Line Timing Taps
E37 thru E52	RAS 0 - RAS 7 Enables
E53 - E54	Force Parity Error ENA
E55 - E56	Write Wrong Parity (Normal)
E56 - E57	Write Wrong Parity (Semi-Disk)
E58 - E59	Disable Refresh

SW3-1	ON = Extended CSR enable OFF= Extended CSR disable
SW3-6	ON = Full 128KW Enabled (Un I/O OFF= Full 128KW Disabled
SW3-7	ON = Enable extended address OFF= Disable extended address

512 KW MOS memory

DIAGNOSTIC ZMSP

SWITCH FUNCTION SUMMARY LIST

S1-1 thru 6	SS-11 Starting Address
S1-6 thru 8 S2-5 and 6	SS-11 Ending Address
S2-1 thru 4	CSR Register Address Select
S2-7	Disable CSR
S2-8	I/O Page Select
S3-1	Enable Extended CSR
S3-2 thru 5	Board Enable
S3-6	Full 512K Board (No I/O Page)
S3-7	4K or 8K I/O Select
S3-8	Disable CSR Bit 14

I/O Page Switch Functions			
	S2-8	S3-6	S3-7
Full 512KW (No I/O Page	0	1	X
4K I/O Page	1	0	1
8K I/O Page	1	0	0
Short Board* (Less than 512KW)	0	0	X

0 = OFF Position
1 = ON position
X = Don't Care

Starting Address	S1-1	S1-2	S1-3	S1-4	S1-5
0KW	0	0	0	0	0
16K	0	0	0	0	1
32K	0	0	0	1	0
48K	0	0	0	1	1
64K	0	0	1	0	0
80K	0	0	1	0	1
96K	0	0	1	1	0
112K	0	0	1	1	1
128K	0	1	0	0	0
144K	0	1	0	0	1
160K	0	1	0	1	0
176K	0	1	0	1	1
192K	0	1	1	0	0
208K	0	1	1	0	1
224K	0	1	1	1	0
240K	0	1	1	1	1
256K	1	0	0	0	0
272K	1	0	0	0	1
288K	1	0	0	1	0
304K	1	0	0	1	1
320K	1	0	1	0	0
336K	1	0	1	0	1
352K	1	0	1	1	0
368K	1	0	1	1	1
384K	1	1	0	0	0
400K	1	1	0	0	1
416K	1	1	0	1	0
432K	1	1	0	1	1
448K	1	1	1	0	0
464K	1	1	1	0	1
480K	1	1	1	1	0
496KW	1	1	1	1	1

0 = OFF Position 1 = ON Position

Ending Address	S1-6	S1-7	S1-8	S2-5	S2-6
0KW	0	0	0	0	0
16K	0	0	0	0	1
32K	0	0	0	1	0
48K	0	0	0	1	1
64K	0	0	1	0	0
80K	0	0	1	0	1
96K	0	0	1	1	0
112K	0	0	1	1	1
128K	0	1	0	0	0
144K	0	1	0	0	1
160K	0	1	0	1	0
176K	0	1	0	1	1
192K	0	1	1	0	0
208K	0	1	1	0	1
224K	0	1	1	1	0
240K	0	1	1	1	1
256K	1	0	0	0	0
272K	1	0	0	0	1
288K	1	0	0	1	0
304K	1	0	0	1	1
320K	1	0	1	0	0
336K	1	0	1	0	1
352K	1	0	1	1	0
368K	1	0	1	1	1
384K	1	1	0	0	0
400K	1	1	0	0	1
416K	1	1	0	1	0
432K	1	1	0	1	1
448K	1	1	1	0	0
464K	1	1	1	0	1
480K	1	1	1	1	0
496K	1	1	1	1	1
512KW	1	1	1	1	1

S3-6 = 1

CSR Address	S2-1	S2-2	S2-3	S2-4
17772100	1	1	1	1
17772102	1	1	1	0
17772104	1	1	0	1
17772106	1	1	0	0
17772110	1	0	1	1
17772112	1	0	1	0
17772114	1	0	0	1
17772116	1	0	0	0
17772120	0	1	1	1
17772122	0	1	1	0
17772124	0	1	0	1
17772126	0	1	0	0
17772130	0	0	1	1
17772132	0	0	1	0
17772134	0	0	0	1
17772136	0	0	0	0

0 = OFF Position 1 = ON Position

NOTE: In Extended Addressing Mode, S3-1 must be set ON.

EXTENDED ADDRESSING

Board Number	S3-2	S3-3	S3-4	S3-5	Memory Bank
0	1	0	0	0	000-512KW
1	0	1	0	0	512-1024KW
2	0	0	1	0	1024-1536KW
3	0	0	0	1	1536-2048KW

NOTE: In Extended Address Mode, S3-1 must be set ON to select each CSR.

256KW MOS memory

DIAGNOSTIC ZMSP

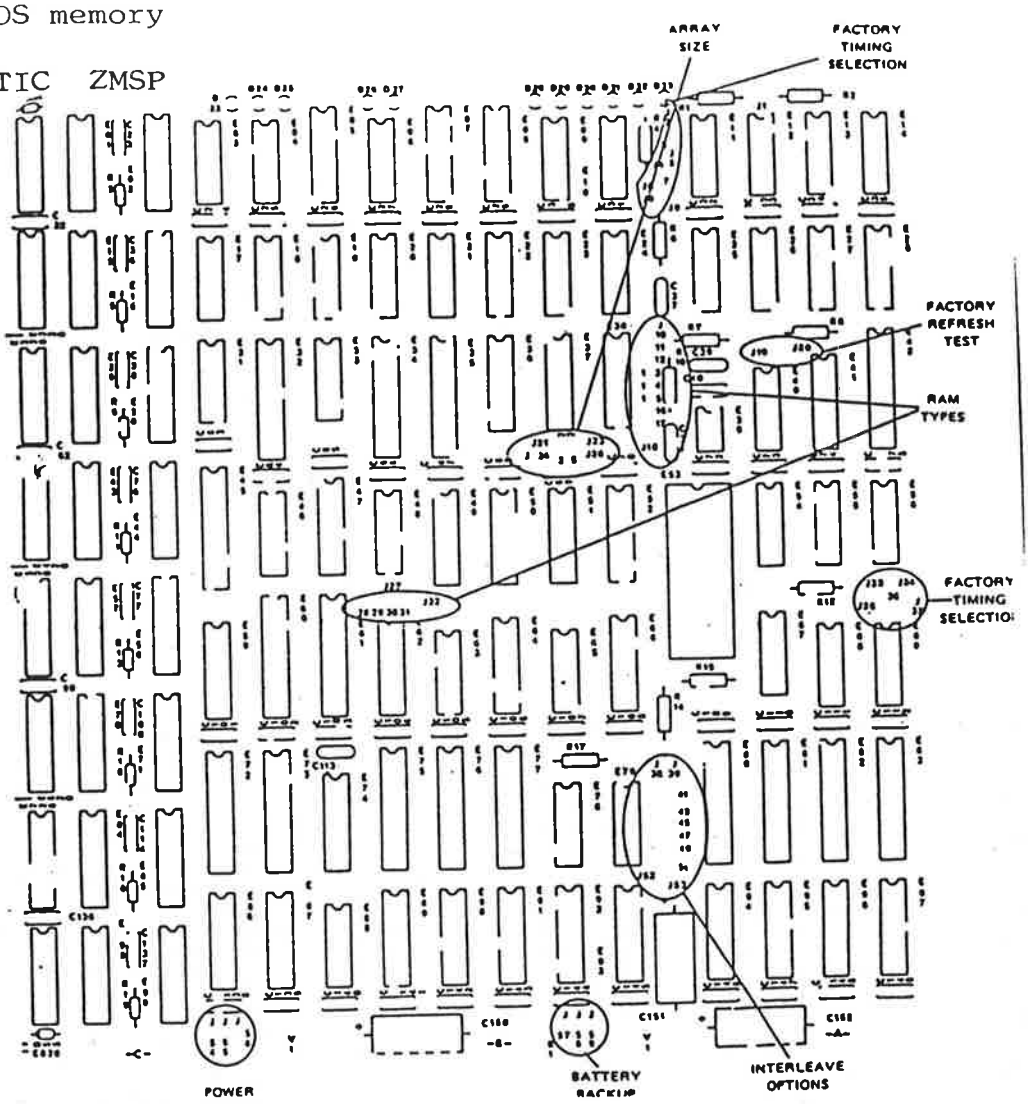


TABLE 3-1 - STARTING ADDRESS SELECT TABLE - MODIFIED UNIBUS

Partial Starting Address		Switch Positions		
Decimal	Octal	ES2-3	ES2-2	ES2-1
0K	SS000000	1	1	1
16K	SS100000	1	1	0
32K	SS200000	1	0	1
48K	SS300000	1	0	0
64K	SS400000	0	1	1
80K	SS500000	0	1	0
96K	SS600000	0	0	1
112K	SS700000	0	0	0

Notes: For SS(two Most Significant Digits of Octal Starting Address), see Table 3-2.

TABLE 3-2 - STARTING ADDRESS SELECT TABLE - EXTENDED UNIBUS

Partial Starting Address		Switch Positions				
Decimal	Octal	ES2-8	ES2-7	ES2-6	ES2-5	ES2-4
0K	00RR0000	0	1	1	1	1
128K	01RR0000	0	1	1	1	0
256K	02RR0000	0	1	1	0	1
384K	03RR0000	0	1	1	0	0
512K	04RR0000	0	1	0	1	1
640K	05RR0000	0	1	0	1	0
768K	06RR0000	0	1	0	0	1
896K	07RR0000	0	1	0	0	0
1024K	10RR0000	0	0	1	1	1
1152K	11RR0000	0	0	1	1	0
1280K	12RR0000	0	0	1	0	1
1408K	13RR0000	0	0	1	0	0
1536K	14RR0000	0	0	0	1	1
1664K	15RR0000	0	0	0	1	0
1792K	16RR0000	0	0	0	0	1
1920K	17RR0000	0	0	0	0	0

Notes: On = 0, Off = 1
For RR (Digits 4 & 5 of Octal Starting Address), see Table 3-1.

TABLE 3-3 - CSR ADDRESS SELECTION

Unibus Address	Special Bus Address	Switch Positions				
		ES0-8 (Disable)	ES0-7 (A04)	ES0-6 (A03)	ES0-5 (A02)	ES0-4 (A01)
772100	177772100	1	0	0	0	0
772102	177772102	1	0	0	0	1
772104	177772104	1	0	0	1	0
772106	177772106	1	0	0	1	1
772110	177772110	1	0	1	0	0
772112	177772112	1	0	1	0	1
772114	177772114	1	0	1	1	0
772116	177772116	1	0	1	1	1
772120	177772120	1	1	0	0	0
772122	177772122	1	1	0	0	1
772124	177772124	1	1	0	1	0
772126	177772126	1	1	0	1	1
772130	177772130	1	1	1	0	0
772132	177772132	1	1	1	0	1
772134	177772134	1	1	1	1	0
772136	177772136	1	1	1	1	1
Disable	Disable	0	X	X	X	X

TABLE 3-4 - RESERVE I/O SPACE

Peripheral Page Size	Unibus Location	Special Bus Location	Switch Positions		
			ES2-8 Special Bus	ES0-2 (A13)	ES0-1 (A12)
2K	126K - 128K	N/A	1	0	0
4K	124K - 128K	N/A	1	0	1
8K	120K - 128K	N/A	1	1	1
2K	N/A	2046K - 2048K	0	0	0
4K	N/A	2044K - 2048K	0	0	1
8K	N/A	2040K - 2048K	0	1	1

NOTE: On = 0, Off = 1

TABLE 3-5 - RAM TYPE JUMPERS

JUMPER	64K	32K				
		-1	-2	-3	-4	
J10 - J11						
J11 - J12						
J12 - J13						
J13 - J14						
J14 - J15						
J15 - J16						
J16 - J17						
J17 - J18						
J27 - J29						
J28 - J29						
J29 - J30						
J30 - J31						
J31 - J32						

NOTE 1 = Jumper Installed

INTERLEAVE					
JUMPER	NON INTL	64K INTL	128K INTL	256K INTL	512K INTL
J38 - J39					
J38 - J40					
J41 - J39					
J42 - J43					
J44 - J45					
J44 - J46					
J45 - J47					
J48 - J49					
J49 - J47					
J50 - J51					
J50 - J52					
J51 - J53					
J52 - J53					
J48 - J46					

128KW MOS memory (MS11-L)

Start/End Address Table #2

"1": ON, "0": OFF

Address			Switch Position				
Decimal	Octal	Start Address	SW1-5	SW1-4	SW1-3	SW1-2	SW1-1
		End Address	SW3-5	SW3-4	SW3-3	SW3-2	SW3-1
SW3	SW1		(BA17)	(BA16)	(BA15)	(BA14)	(BA13)
4K	0K	S S 0 0 0 0 0 0 0	0	0	0	0	0
8K	4K	S S 0 0 0 0 0 0 1	0	0	0	0	1
12K	8K	S S 0 0 0 0 0 1 0	0	0	0	1	0
16K	12K	S S 0 0 0 0 0 1 1	0	0	0	1	1
20K	16K	S S 0 0 0 0 1 0 0	0	0	1	0	0
24K	20K	S S 0 0 0 0 1 0 1	0	0	1	0	1
28K	24K	S S 0 0 0 0 1 1 0	0	0	1	1	0
32K	28K	S S 0 0 0 0 1 1 1	0	0	1	1	1
36K	32K	S S 0 0 0 1 0 0 0	0	1	0	0	0
40K	36K	S S 0 0 0 1 0 0 1	0	1	0	0	1
44K	40K	S S 0 0 0 1 0 1 0	0	1	0	1	0
48K	44K	S S 0 0 0 1 0 1 1	0	1	0	1	1
52K	48K	S S 0 0 0 1 1 0 0	0	1	1	0	0
56K	52K	S S 0 0 0 1 1 0 1	0	1	1	0	1
60K	56K	S S 0 0 0 1 1 1 0	0	1	1	1	0
64K	60K	S S 0 0 0 1 1 1 1	0	1	1	1	1
68K	64K	S S 0 0 1 0 0 0 0	1	0	0	0	0
72K	68K	S S 0 0 1 0 0 0 1	1	0	0	0	1
76K	72K	S S 0 0 1 0 0 1 0	1	0	0	1	0
80K	76K	S S 0 0 1 0 0 1 1	1	0	0	1	1
84K	80K	S S 0 0 1 0 1 0 0	1	0	1	0	0
88K	84K	S S 0 0 1 0 1 0 1	1	0	1	0	1
92K	88K	S S 0 0 1 0 1 1 0	1	0	1	1	0
96K	92K	S S 0 0 1 0 1 1 1	1	0	1	1	1
100K	96K	S S 0 0 1 1 0 0 0	1	1	0	0	0
104K	100K	S S 0 0 1 1 0 0 1	1	1	0	0	1
108K	104K	S S 0 0 1 1 0 1 0	1	1	0	1	0
112K	108K	S S 0 0 1 1 0 1 1	1	1	0	1	1
116K	112K	S S 0 0 1 1 1 0 0	1	1	1	0	0
120K	116K	S S 0 0 1 1 1 0 1	1	1	1	0	1
124K	120K	S S 0 0 1 1 1 1 0	1	1	1	1	0
128K	124K	S S 0 0 1 1 1 1 1	1	1	1	1	1

1. Octal SS is decided by SW1, SW3, 6 to 9
2. Decimal address is only when SS=00.
3. SW1-1 to SW1-5 : for Start Address
   SW3-1 to SW3-5 : for End Address

Start/End Address Table #1

"1": ON, "0": OFF

Address			Switch Position			
Decimal	Octal	Start Address	SW1-9	SW1-8	SW1-7	SW1-6
		End Address	SW3-9	SW3-8	SW3-7	SW3-6
			BA-21	(BA-20	(BA-19)	(BA-18)
0K	0 0 R R 0 0 0 0		0	0	0	0
128K	0 1 R R 0 0 0 0		0	0	0	1
256K	0 2 R R 0 0 0 0		0	0	1	0
384K	0 3 R R 0 0 0 0		0	0	1	1
512K	0 4 R R 0 0 0 0		0	1	0	0
640K	0 5 R R 0 0 0 0		0	1	0	1
768K	0 6 R R 0 0 0 0		0	1	1	0
896K	0 7 R R 0 0 0 0		0	1	1	1
1024K	1 0 R R 0 0 0 0		1	0	0	0
1152K	1 1 R R 0 0 0 0		1	0	0	1
1280K	1 2 R R 0 0 0 0		1	0	1	0
1408K	1 3 R R 0 0 0 0		1	0	1	1
1536K	1 4 R R 0 0 0 0		1	1	0	0
1664K	1 5 R R 0 0 0 0		1	1	0	1
1792K	1 6 R R 0 0 0 0		1	1	1	0
1920K	1 7 R R 0 0 0 0		1	1	1	1

1. Octal RR is decided by SW1, SW3 (1-5) (Table #2)
2. Decimal address is only when RR=00
3. SW1-6 ~ SW1-9 : for Start Address
   SW3-6 ~ SW3-9 : for End Address

10-2 Reserved I/O Function

8K words, 4K words, or 2K words can be set on upper address as address space for I/O device by setting SW2-6~10 as follows.

* I/O Space Address Table

I/O SIZE	18 Bit Address line	22 Bit Address line	SW2-9	SW2-8 (Memory Mgt-Used)	SW2-7 (BA12)	SW2-6 (BA13)
2K	126K ~ 128K	———	0	1	1	1
4K	124K ~ 128K	———	0	1	0	1
8K	120K ~ 128K	———	0	1	0	0
2K	———	2046K ~ 2048K	1	1	1	1
4K	———	2044K ~ 2048K	1	1	0	1
8K	———	2040K ~ 2048K	1	1	0	0

"1": ON, "0": OFF

10-3 Parity Control Function

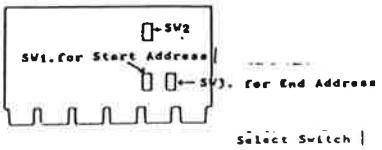
The parity will be automatically generated on a WRITE operation (DATO, DATOB) and will be checked on a READ operation for each byte by parity control function on the module.

When an error is detected, the error information will be sent to the processor, and the on board parity LED (red) will be on.

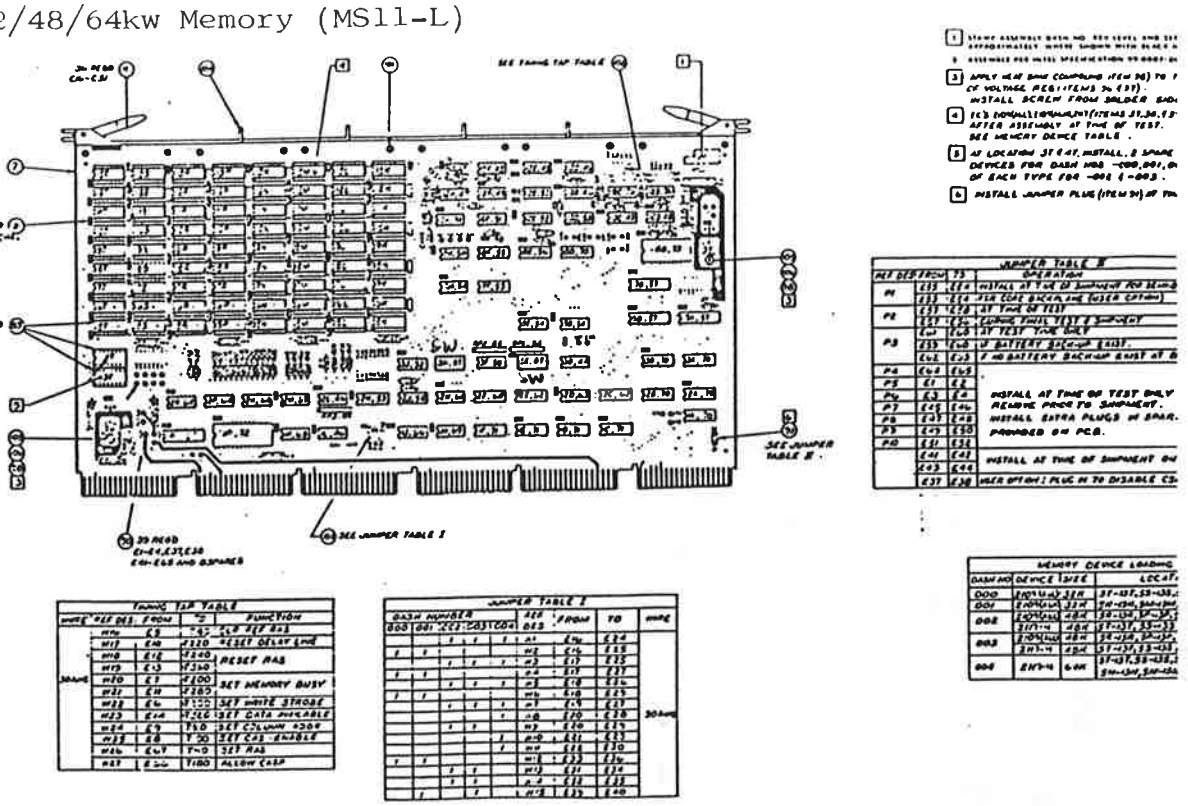
C. S. R. Address Table

"1": ON, "0": OFF, X: Irrevant

18 Bit Address line	22 Bit Address line	SW2-5 (Disable)	SW2-4 (BA04)	SW2-3 (BA03)	SW2-2 (BA02)	SW2-1 (BA01)
772100	17772100	0	1	1	1	1
772102	17772102	0	1	1	1	0
772104	17772104	0	1	1	0	1
772106	17772106	0	1	1	0	0
772110	17772110	0	1	0	1	1
772112	17772112	0	1	0	1	0
772114	17772114	0	1	0	0	1
772116	17772116	0	1	0	0	0
772120	17772120	0	0	1	1	1
772122	17772122	0	0	1	1	0
772124	17772124	0	0	1	0	1
772126	17772126	0	0	1	0	0
772130	17772130	0	0	0	1	1
772132	17772132	0	0	0	1	0
772134	17772134	0	0	0	0	1
772136	17772136	0	0	0	0	0
Disable	Disable	1	X	X	X	X



INTEL 32/48/64kw Memory (MS11-L)



2.5 CARD SELECT PROGRAMMING

Dual-in-line package (DIP) switches, S1 and S2, on each memory card, allow easy selection of the desired UNIBUS address range. The unique card select address must be entered by means of these DIP switches to implement proper memory operation. The OPEN position of the switches is marked on the switch packages, as shown in Figure 2-2.

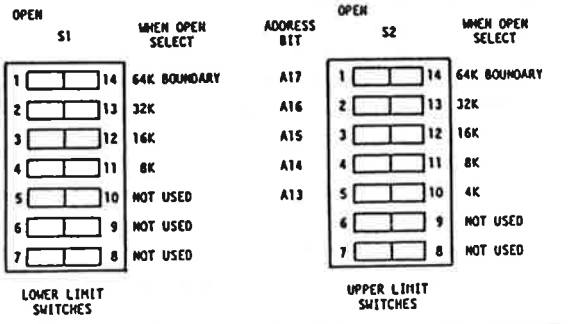


Figure 2-2. Card Select Switches

Switch S1 allows the user to set the lower address limit, or the starting address, for the memory card. The lower limit is relative to the address position of the memory card in the overall system (Table 2-6). If the lower limit is '0', all switch contacts are closed. If the lower limit is 8K, contacts 4-11 are open and the others closed, etc. Starting addresses are partitioned on 8K boundaries.

Switch S2 sets the upper address limit, or ending address, for each memory card. Table 2-6 indicates switch settings for a 128K system. Ending addresses are partitioned on 4K boundaries. Section 5.6 gives further examples of switch settings.

CAUTION

Improper switch settings are a frequent cause of memory failure.

It is also recommended that memory card assignments be recorded in Table 2-7 with memory capacity, and starting and ending addresses for each location in the backplane.

Table 2-6. Switch Settings for Lower and Upper Memory Limits, and Octal Addresses

SWITCH	STARTING ADDRESS DATA: S1					ENDING ADDRESS DATA: S2						
ADDRESS	17	16	15	14	STARTING ADDRESS	OCTAL STARTING ADDRESS	17	16	15	14	13	ENDING ADDRESS	OCTAL ENDING ADDRESS
CONTACT	1	2	3	4			1	2	3	4	5		
	0	0	0	0	0	000000	0	0	0	0	0	4K-1	017777
							0	0	0	0	1	8K-1	037777
	0	0	0	1	8K	040000	0	0	0	1	0	12K-1	057777
							0	0	0	1	1	16K-1	077777
	0	0	1	0	16K	100000	0	0	1	0	0	20K-1	117777
							0	0	1	0	1	24K-1	137777
	0	0	1	1	24K	140000	0	0	1	1	0	28K-1	157777
							0	0	1	1	1	32K-1	177777
	0	1	0	0	32K	200000	0	1	0	0	0	36K-1	217777
							0	1	0	0	1	40K-1	237777
	0	1	0	1	40K	240000	0	1	0	1	0	44K-1	257777
							0	1	0	1	1	48K-1	277777
	0	1	1	0	48K	300000	0	1	1	0	0	52K-1	317777
							0	1	1	0	1	56K-1	337777
	0	1	1	1	56K	340000	0	1	1	1	0	60K-1	357777
							0	1	1	1	1	64K-1	377777
	1	0	0	0	64K	400000	1	0	0	0	0	68K-1	417777
							1	0	0	0	1	72K-1	437777
	1	0	0	1	72K	440000	1	0	0	1	0	76K-1	457777
							1	0	0	1	1	80K-1	477777
	1	0	1	0	80K	500000	1	0	1	0	0	84K-1	517777
							1	0	1	0	1	88K-1	537777
	1	0	1	1	88K	540000	1	0	1	1	0	92K-1	557777
							1	0	1	1	1	96K-1	577777
	1	1	0	0	96K	600000	1	1	0	0	0	100K-1	617777
							1	1	0	0	1	104K-1	637777
	1	1	0	1	104K	640000	1	1	0	1	0	108K-1	657777
							1	1	0	1	1	112K-1	677777
	1	1	1	0	112K	700000	1	1	1	0	0	116K-1	717777
							1	1	1	0	1	120K-1	737777
	1	1	1	1	120K	740000	1	1	1	1	0	124K-1	757777
							1	1	1	1	1	128K-1	777777

0 = Closed Switch Contact; 1 = Open Switch Contact.

Control Status Register Operations (Continued)

All CSR's have a pre-determined address. The CSR address of each in-5034 memory board is determined by its starting address set by the on-board lower limit DIP switch, S1, as shown in Table 3-2.

Table 3-2. Control Address Register Addresses

STARTING ADDRESS OF MEMORY	CSR ADDRESS IN OCTAL	STARTING ADDRESS OF MEMORY	CSR ADDRESS IN OCTAL
0	772100	64K	772120
8K	772102	72K	772122
16K	772104	80K	772124
24K	772106	88K	772126
32K	772110	96K	772130
40K	772112	104K	772132
48K	772114	112K	772134
56K	772116	120K	772136

Table 1-1. Memory Configurations

MEMORY SIZE (CAPACITY)	32K		48K		64K
MEMORY CHIP	8K L NO JUMPER E39 to E40	8K U JUMPER E39 to E40	8K L and 16K	8K U and 16K	16K
ASSEMBLY 05-0787 VARIATION (DASH NO)(2)	-000	-001	-002	-003	-004

SECTION 6

DISC CONTROLLERS FOR DEC

In the decade since DEC introduced the PDP-11, peripheral controller manufacturers have mushroomed to provide DEC users with system enhancement products. Ken Simmons, director of systems engineering for MDB Systems, headquartered in California, writes about the disc controller market as it relates to Digital products.

Historically, DEC has left the door open for 'compatible' manufacturers who could emulate proprietary controllers for devices different from those of DEC itself. The current disc controller market is an example.

DEC provides only a 10M byte drive (RL02) for its popular LSI-11 series of computers. This offers a minuscule amount of memory for a disc drive. By comparison, larger systems such as the 11/70 and VAX series have disc drive subsystems with capacities in the hundreds of megabytes range.

By adopting Control Data Corporation's storage module drive interface (SMD) for its larger systems, DEC almost single-handedly made it the industry standard. Now about 80% of the manufacturers who offer disc drives emulate CDC's drive so that their products will be DEC compatible.

DEC's high end systems, however, represent a minority of their system sales. The LSI-11 and PDP-11 populations far outnumber those of their larger counterparts and are sometimes seemingly orphaned by DEC and in need of enhancement.

Companies like MDB have made a market and technological impact by catering to LSI-11 and PDP-11 enhancement requirements.

One of its major projects at the moment is migrating the RM series of DEC disc drives into Q-bus systems, thereby substantially enhancing the DEC supplied capability.

Aiding their effort is the explosion of SMD-compatible devices that manufacturers throughout the world are supplying. Although CDC set the standard with the original storage module drive, many manufacturers are providing similar drives with variations of capacity and price.

Up to now the biggest problem has been one of controllers to accommodate drive technology. It has advanced so quickly that the user has become frustrated by being unable to select one of the new products because it would require shutting down a system to reconfigure a new drives's parameters.

Controllers are now being introduced with an automatic configuration feature which renders obsolete that concern. less than one year ago a controller came with a single set of chips to handle a particular manufacturer's drive. Some new controller technology uses firmware to accommodate up to eight different types and manufacturers of disc drives without reprogramming. And, should the user desire a drive that is not one of the programmed eight, all that is required is to replace a PROM with the new driver's parameters written on it (rather than on the disc itself).

This automatic configuration feature allows the user to take immediate advantage of economic benefits or technological breakthroughs by drive manufacturers as they occur.

One controller, the MLSI RM-11, is able to emulate DEC's RM02, RM03, RM05 and RK06/RK07 drives. The important point is that it is driver and diagnostic transparent to all DEC operating systems (plus UNIX and TSX) while maintaining true media compatibility with DEC RM series drives.

By simultaneously mixing emulation modes, any combination of two fixed or removable disc drives can be supported by such a controller. Another trend is illustrated by its maximum capacity of 512M byte per formatted device, designed to increase along with disc technology.

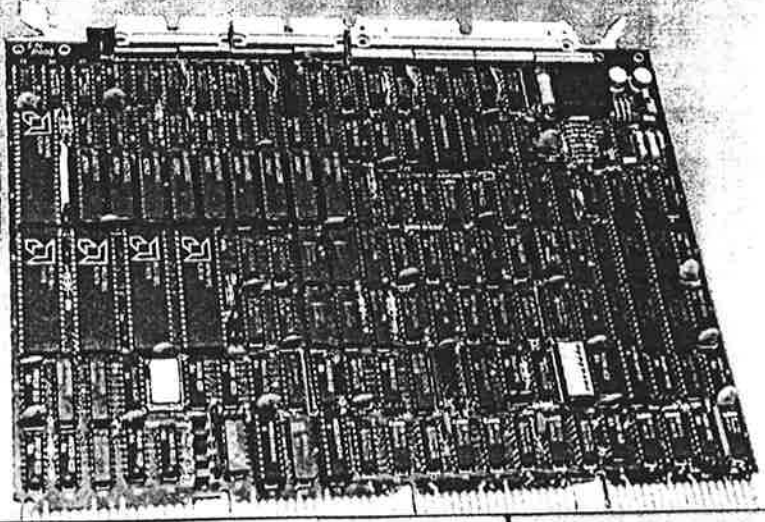
Sophisticated user options are now often included, such as selectable 16, 18 and 22 bit addressing, four-level priority, and interrupt vectors. Another useful operating mode is a DMA throttle which allows data transfer bursts from 1-16 words. This controller also includes a DEC-compatible firmware bootstrap to handle both RM and RK series drives. Other important characteristics include DEC-compatible 32 bit data error correction code as well as bit header CRC and media defect flagging. Multiple sector buffering can be used to eliminate 'data-late' errors.

In practice, the controller's firmware interrogates a switch for information regarding the disc drive types in use. The controller then automatically structures its firmware to identify the drives by number of cylinders, sectors and heads as well as number of blocks in each logical unit.

Future disc technology advances are handled by changing one PROM rather than entire firmware PROM sets. Important, too, is that the media compatibility feature means that all modifications, now or in the future, are accommodated by writing on the PROM, not the disc. Nothing goes directly on the header, because many users feel the practice is too risky.

Another tendency is the use of the controller to reconfigure device addressing. Called 'address mapping', the controller does all the address conversion without affecting the operating system. Such a product is transparent to the host manufacturer's diagnostics and drives for the operating systems. ■

The reconfigurable MLST RM-11 disc controller



DISCS

DEVICE/CONTROLLER	MODULE	DESCRIPTION	LOCATION	BOOT MNEMONIC
RK05/RK11-D	M7257 M7256 M7255 M7254	BUS CONTROLLER DATA PATH DISC CONTROLLER STATUS CONTROL BACKPLANE	C-F 4 " 3 " 2 " 1	DK
RK11-C				
RK06/7 RK611	M7900 M7901 M7902 M7903 M7904	UNIBUS I/O REGISTER CONTROL DATA PATH DISC CONTROL BACKPLANE	A-F 8 7 6 5 4	DM
RL01/2 RL11	M7762	CONTROLLER	A-F 3-8	DL
RX01 RX11	M7846	CONTROLLER	C-F 3-8	DX
RX02 RX211	M8256	CONTROLLER	C-F 3-8	DY

FIGURE 1-1
DEC UNIBUS DISK SUBSYSTEMS

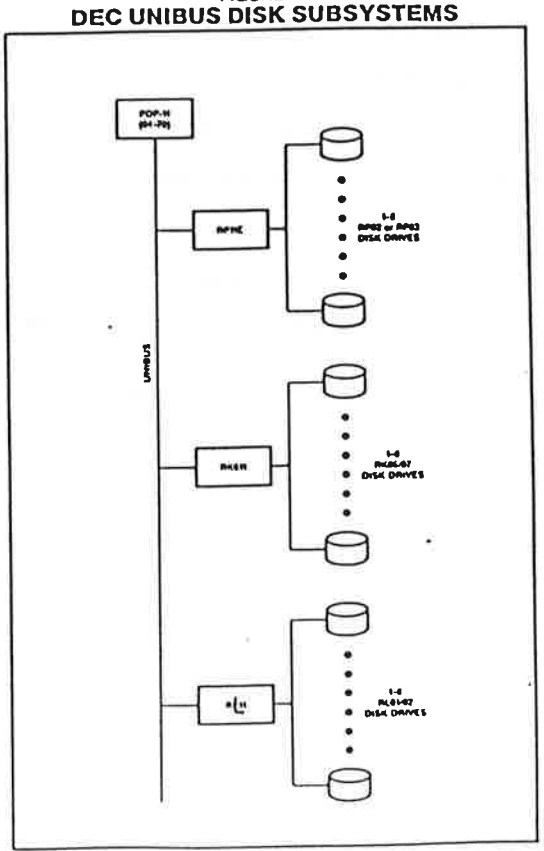
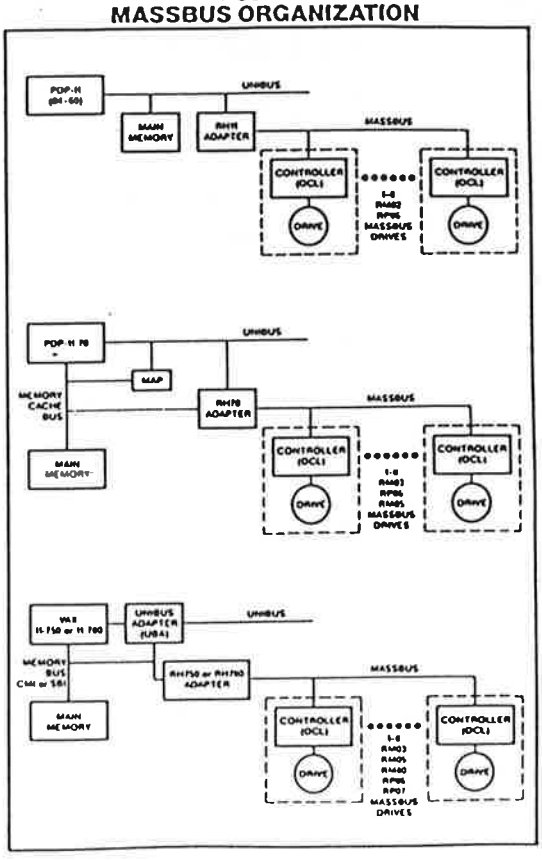


FIGURE 1-2
MASSBUS ORGANIZATION



DRIVE/CONTROLLER COMPARISON CHART

DRIVE & MNEMONIC		CONTROLLER	NOTES
RA60	DU	UDA 50	205 Mb Pack
RA80, RA81	DU	UDA 50	121/456 Mb Winchester
RK05 (F)	DK	RK11, RKV11	2.5 (5.0) Mb Cartridge
RK06, RK07	DM	RK611, RK711	14/28 Mb Cartridge
RL01, RL02	DL	RL11, RKV11	5.2/10.4 Mb Cartridge
RM02, RM03, RM05	DR	RH11, RH70	67/256 Mb Pack
RM80	DR	RH11, RH70	124 Mb Winchester
RP02, RP03	DP	RP11	20/40 Mb Pack
RP04, RP05, RP06	DB	RH11, RH70	88/176 Mb Pack
RS03, RS04	DS	RH11, RH70	¼/½ Mb Fixed Head
RS11	DF	RF11	¼ Mb Fixed Head
RS64		RC11	160 Kb Fixed Head
RX01	DX	RX11, RXV11	¼ Mb Floppy
RX02	DY	RX211, RXV21, RXC11	½ Mb Floppy
PC05	PC	PC11	Paper Tape Reader Punch
TS11	MS	Module M7983	24"/1600 bpi R-R
TS03	MT	TM11, TMA-11, TMB-11	7"/800 bpi R-R
TE10, TU10	MT	TM11, TMA-11, TMB-11	24"/1600,800 bpi R-R
TE16, TU16	MM	TM02, TM03, RH11, RH70	24"/1600,800 bpi R-R
TU45, TU77	MM	TM03, RH11, RH70	24"/1600,800 bpi R-R
TJ55, TU56	DT	TC11	DECtape I R-R (½" width)
TU58	DD	RS-422/423/232-C, DL11	DECtape II ½ Mb Cartridge
TU60	CT	TA11	Cassette
TSV05			24"/1600 bpi Self Loading R-R
	TR	TR79F	PDP-11 to Hewlett Packard 7970-E MTU

Note:

R-R = Reel to Reel

DEC DISC DRIVES

	RKO5	RKO6	RKO7	RLO1	RLO2	RPO2	RPO3	RPO4	RPO5	RPO6	RPO7	RMO2	RMO3	RMO5	RM80
DISC DRIVE	FRONT CARTRIDGE	TOP CARTRIDGE	TOP CARTRIDGE	TOP CARTRIDGE	TOP CARTRIDGE	DSU	DSU	DSU	DSU	DSU	WINCHESTER	SMD	SMD	SMD	WINCHESTER
MANUFACTURER MODEL	DEC -	DEC -	DEC -	DEC -	DEC -	MEMOREX 660 CDC 9742	CDC 9746	MEMOREX ?	MEMOREX ?	MEMOREX 677		CDC 9762	CDC 9762	CDC 9766	
DATA SURFACES HEADS CYLINDERS TRACKS SECTORS	2 2	3 4	3 4	2 2 256 40	2 2 512 40		20 20 406 20 10	19 20 411 19 22	19 20 411 19 22	19 20 823 19 22	16 33 630 32 50	5 6 823 5 32	5 6 823 5 32	19 20 823 19 32	7 15 1118 - 32
INTERFACE (DEC)	RK11-D	RK611	RK611	RL11	RL11	RP11	RP11	RH11	RH11	RH11	VAX	RH11	RH11	RH11	VAX
SYSTIME	S5300 S5301					S5310	S5310					S5311	S5311		
SYSTEMS INDUSTRIES												SI9400	SI9400	SI9400	
EMULEX												SC11	SC11	SC11	
MINI COMPUTER TECHNOLOGY												SMC11	SMC11	SMC11	
FORMATTED CAPACITIY UNFORMATTED CAPACITIY	2.5/5.0	14MB	28MB	5.2	10.4MB	 20MB	 40MB	88MB 100MB	88MB 100MB	176MB 200MB	516MB	67MB 80MB	67MB 80MB	276MB 300MB	124MB
BOOT MNEMONIC	DK	DM	DM	DL	DL	DP	DP	DB	DB	DB	DB	DR	DR	DR	DR

S.M.D.

STORAGE MODULE DRIVE:

CDC	9760	9762	9766
CAPACITY	40MB	80MB	300MB
CYLINDERS	411	823	823
PACK	9876	9877	9883
DEC	-	RM02/03	RM05

CONTROLLER		EMULATION	SIZE
RH11/RH70		RM02/03/05	
SYSTIME 5311		RP02/03	QUAD x 4 + B/PLANE
EMULEX SC11	A	RP02/03	1QUAD 1 HEX
	B	RM02/03/05	
	C	RK06/7	
	L	RL02	
EMULEX SC21	"		1 HEX
EMULEX SC12	"		1 QUAD

SYSTEMS INDUSTRIES SI9400 RM02/3/5

MCT SMC11	NONE
SMV11	"

C.M.D.

CARTRIDGE MODULE DRIVE — CDC 9448

Formatted Capacity (Total) 32 / 64 / 96 } M Bytes : Dependant on heads installed

Formatted Capacity (Cartridge) 16 M Bytes (1 Servo Surface)

Formatted Capacity (Fixed Module) 16 M Bytes per surface
3 Fixed Platters
5 Data Surfaces 1 Servo Surface

CONTROLLER	EMULATION	SIZE
DILOG 200	RK05	QUAD
DILOG 202	RP02/03	QUAD
DILOG 202A	RK06	QUAD
EMULEX SC01 A/C	RP03/RK06	2 x QUAD
EMULEX SC02 A/C	RP03/RK06	QUAD

CDC DISC DRIVES

MODEL	9742	9746	9747	9760	9762	9766	9448
DEC MODEL	RP02	RP03	RP03	NONE (EMULATES RP03)	RM02/03	RM05	NONE (EMULATES RK05/ 06/RM03)
CAPACITY	20MB	40MB	40MB	40MB	80MB	300MB	32/63/96MB
PLATTERS	11	11	11		3	10	3 FIXED 1 CARTRIDGE
DATA SURFACES	20	20	20		5	19	6
HEADS	20	20	20		6	20	8
CYLINDERS		406	406		823	823	823
TRACKS		20	20		5	19	6
SECTORS		10	10		32	32	VARIABLE
	DSU	DSU	DSU	SMD	SMD	SMD	SMD

SMD CONTROLLERS

CONTROLLER	DISC SYSTEM	EMULATION	DIAGNOSTICS
SYSTIME 5311	CDC 9760/9762	RPO2/03	SMD DIAGNOSTICS RUN UNDER RSTS/E AT OPTION LEVEL AS STAND ALONE PROGRAM ACCOUNT 0, 1 DIAGNOSTICS : ZRPSMD - RELIABILITY ZRPSMM - MULTIDISC FORMATTING : DONE UNDER COPY PROGRAM
MINI COMPUTER TECHNOLOGY SMC-11 SMV15	CDC 9760/9762/9766 9448, FUJITSU/KENNEDY " " "	NOT A TRUE EMULATION OF ANY DEC SYSTEM " " "	FORMATTING AND DIAGNOSTICS : SMCFA3 INCLUDES FORMAT PROGRAM AND VARIOUS TEST PROGRAMS TO RUN THE DRIVES. THE SMC11 IS UNIBUS ONLY, SMV11 IS BOTH UNIBUS AND MASSBUS
EMULEX SCXX/A SCXX/B1 SCXX/B2 SCXX/C	CDC 9760/9762 " " CDC 9766 " "	RPO20/3 RMO2/03 RPO6 RKO6	ZRP ??? PATCHES ARE REQUIRED TO RUN TESTS ZRM ??? " " " " " ZR6 ??? " " " " "
SYSTEMS INDUSTRIES SI 9400	CDC 9762/9766	RMO2/03/05	NEW 94 : CONTROLLER DIAGNOSTICS THE SYSTEM WILL ALSO RUN ALL DEC DIAGNOSTICS THAT DO NOT REQUIRE A MAINTENANCE REGISTER

D I S C P A C K S

Bin	Type	Used on	Sectors	TPI	BPI
5624	2315 Front Load	D400/Series 30	8	100	1100
6115	CE Pack 2315 Front Load	D400	(Low Density)		1100
5625	2315 Front Load	D800	16	200	2200
6219	CE Pack 2315 Front Load	D800/RK05/Pertec	(High Density)		2200
5627	5440 Top Load	D818	16	100	2200
6205	CE Pack Top Load	D818/D1600/44B/Hawk/Pertec		200	2200
5626	5440 Top Load	D1600	16	200	2200
6111	CE Pack 89259000 11 High	MEM660/CDC 9742/(RP02)			
31244	2316 Top Load 11 High	CDC 9746/(RP03)	20	200	2200
6224	CE Pack Top Load 11 High	CDC 9746/7/D3200/D8000			
6282	2316 Top Load 11 High	CDC 9747/D3200/D8000	32	200	2200
6298	80MB 5 High 70438000 9877	CDC 9762/(SMD)			
6297	CE Pack Top Load 5 High 70438700	CDC 9762/(SMD) 9775-51			
37263	CE Pack 91204-51	CDC 9448/(CMD)			
37043	Data Pack 1204-G300	CDC 9448/(CMD)			
34222	CE Pack 9883-51 7043003	CDC 9766/(SMD)			
34223	300MB 9883 70430505	CDC 9766/(SMD)			
35068	CE Pack 9876-51 70439001	CDC 9760/(SMD)			
35069	40MB 9876 70439500	CDC 9760/(SMD)			
6337	RL01DC	DEC RL01			
33667	Disc Cartridge RL02K-DC (Data)	RL02	40		
5916	2315 Front Load	DEC RK05/PDP11	12	200	00
6338	Twin Disc Top Load	DEC RK06	12		
35333	Twin Disc Top Load RK07K-DC	DEC RK07			
6331	CE Pack RK06K-AC	DEC RK06			
33591	CE Pack RK07K-AC	DEC RK07			
6280	5440 Top Load	Pheonix/C.A. Pertec/LSI 11	12	200	2200
6288	2315 Front Load	Pertec	24	200	220
6300	Fixed Platter (CDC 89293100)	Pertec 5/10 MB/D818/44B			
6329	5440 Top Load	Diablo 44B	24	200	2200
6138	CE Pack EDS 8				
6249	CE Pack 100 MB				
6262	CE Pack 3330 IBM Model II				
6377	CE Pack Multi Platter	Calcomp 114 (GTE)			
38253	CE Pack TD278	DRI			
31646	CE Pack 12541-001	Calcomp T50			
33079	CE 880-51				

RKO5 - J	EXCHAGABLE	2.4 M BYTE
RKO5 - F	FIXED	4.8 M BYTE

1) Switch on mains power

2) Check that power indicator and Load Lamps are illuminated

3) Install Disc

4) Press Load/Run and write protect

5) Wait for ready and on Cylinder indicators to light

6) Boot device using Consol emulator DK CR or Toggle in Bootstrap routine

7) NEVER Remove power from the system with the Heads Loaded

8) Set Load/Run switch to Load

9) Wait for Load Lamp to light

10) Remove Disc

11) Base Address : 777400

12) Vector Address : 220 BR: 5

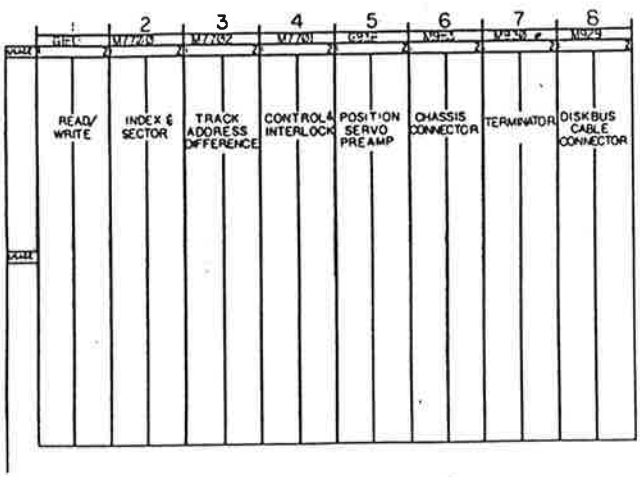
13) Controller : RK11-D 7254, 55, 56, 57

Fixed Disc allways set on an even device boundary DK2: and DK3: at T.S.C.

14) RK11 uses a 4 slot dedicated backplane.

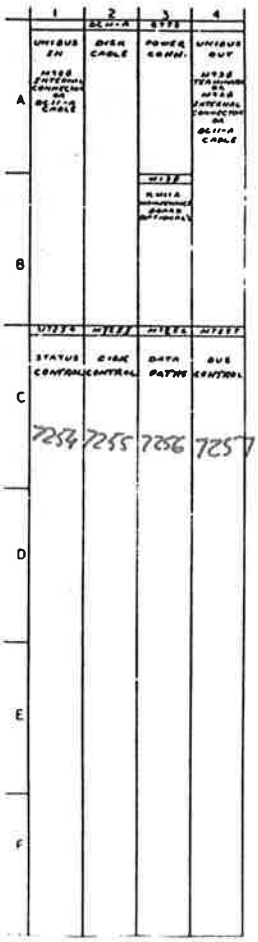
R.K.

ZRKHF0	RK 11/RK 05 Performance Exerciser
ZRKIAS	RK 11/RK 05 Utility Package
ZRKJD0	RK 11/RK 05 Basic Logic Test 1
ZRKKD0	RK 11/RK 05 Basic Logic Test 2
ZRKLD0	RK 11/RK 05 Dynamic Test



RK05 LOGIC CAGE.

RK11



RK11 DISK SYSTEM

3 TYPES OF CONTROLLER

1. RK11C - SSI Contained on many cards.
2. RK11D - MSI Contained on 4 cards.
3. RK11E - Same as RK11D, but 18 bits.

DISC DRIVE

RK05 - uses IBM 2315 disc cartridges.
- 2 surface.
- 203.
- 12 sectors.
- 400_8 or 256_{10} words/sector.
- upto 8 drives/controller.

SECTOR FORMATE

PREAMBLE	SYNC BIT	HEADER	DATA	CHECKSUM	POSTAMBLE
15_8 WORDS OF ZEROS		CYLINDER ADRS 1 WORD	$256_{10}(400_8)$ WORDS (16-BITS OR 18-BITS)	SECTOR CHECKSUM 1 WORD	1 WORD OF ZEROS

The preamble and postamble areas of a sector serve as boundaries before and after information major states (HEADER, DATA, CHECKSUM) to ensure campatibility between disc drives due to variations in sector pulse positioning.

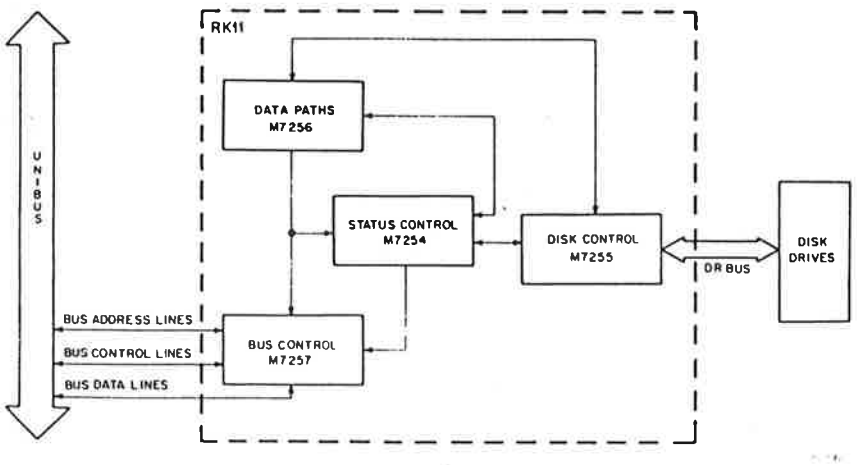


Figure 1-2. RK11 Controller Functional Block Diagram

OPERATING INSTRUCTIONS FOR RX02

1. Ensure power switch at rear of unit is ON

2. Place Diskettes in slots with the label facing up and on the right. At rear of Diskette.

3. Press down Covers until they latch into position.

NOTE

DO NOT leave diskette in unit when applying or removing power as this may corrupt data on diskette.

4. Boot device via consol emulator (RX01 = DX) RX02 = DY) or toggle in bootstrap routine.

BASE ADDRESS: 777170

VECTOR ADDRESS: 264

CONTROLLER: RX01 = RX11 = M7864 - Non DMA Device

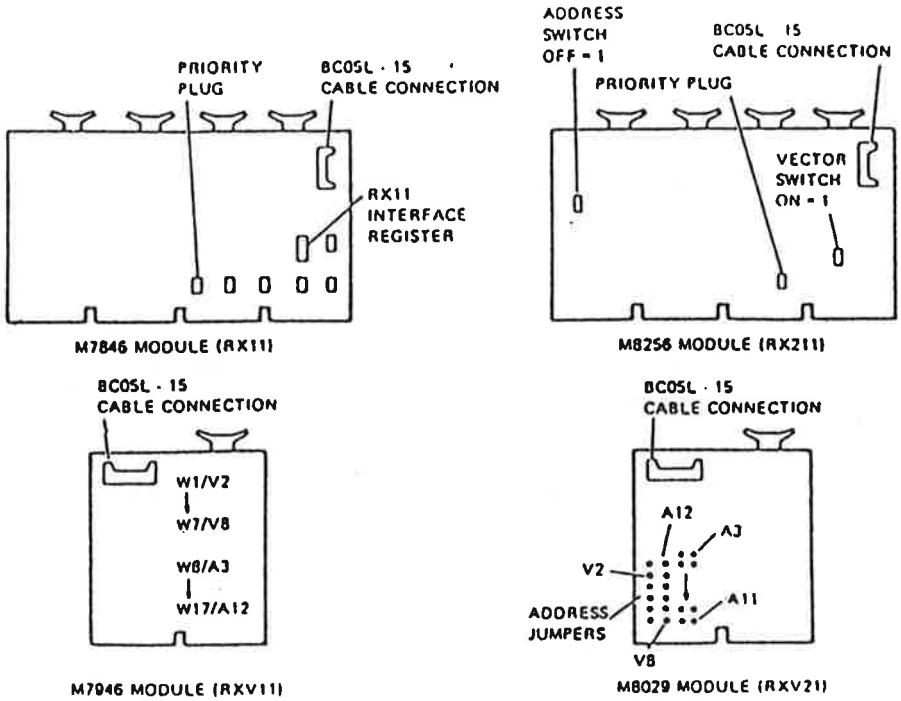
: RX02 = RX211 = M8256 - DMA Device

Install into any Quad HT S.P.C. Slot.

Diagnostics

ZRXA(x) system reliability test
ZRXB(x) interface diagnostic* } RX01

ZRXD(x) RX02 performance exerciser
ZRXF(x) RX02 function/logic
ZRXC(x) RX02 utility driver (Brutus)
ZRXE(x) RX02 formatter program*



PDP-11 (M7846) (M8256)

BR Priority	*Unibus Address 17717X		*Vector Address (264g)	
BR7 – 54-08782	A12/W18 – Removed	SW1 OFF	V2/W1 – Installed	SW1 ON
BR6 – 54-08780	A11/W17 – Removed	SW2 OFF	V3/W2 – Removed	SW2 OFF
*BR5 – 54-08778	A10/W16 – Removed	SW3 OFF	V4/W3 – Installed	SW3 ON
BR4 – 57-08776	A9/W15 – Removed	SW4 OFF	V5/W4 – Installed	SW4 ON
	A8/W14 – Installed	SW5 ON	V6/W5 – Removed	SW5 OFF
	A7/W13 – Installed	SW6 ON	V7/W6 – Installed	SW6 ON
	A6/W12 – Removed	SW7 ON	V8/W7 – Removed	SW7 OFF
	A5/W11 – Removed	SW8 OFF		
	A4/W10 – Removed	SW9 OFF		
	A3/W9 – Removed	SW10 OFF		

LSI-11 (M7946) (M8029)

*Register Address (17717X)	*Vector Address (264g)
A12 – Installed	V2 – Installed
A11 – Installed	V3 – Removed
A10 – Intalled	V4 – Installed
A9 – Installed	V5 – Installed
A8 – Removed	V6 – Removed
A7 – Removed	V7 – Installed
A6 – Installed	V8 – Removed
A5 – Installed	
A4 – Installed	
A3 – Installed	

*Standard

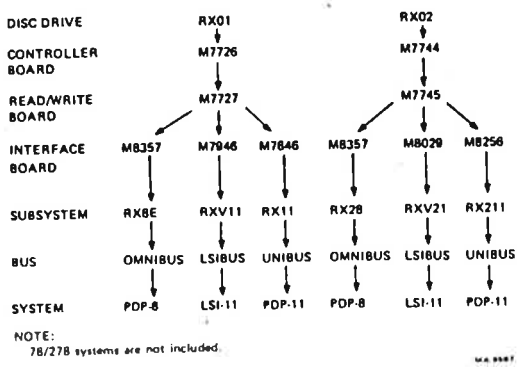


Figure 1-1 What System/Subsystem Is This?

RL01	EXCH DISC	5.2 M BYTES
RL02	" "	10.4 M BYTES

1) Close mains Cct Breaker on Rear of Drive.

2) Wait for Load Lamp to illuminate.

3) Raise Cartridge access cover.

4) Load Disc.

5) Shut access cover.

6) Press write protect.

7) Press Load.

8) Load lamp will go out, the drive will run up; approx 30 sec the heads load and the READY lamp is illuminated.

9) Boot device VIA Consol Emulator DL CR or a toggle in Bootstrap routine.

10) NEVER remove power with the Head Loaded.

11) Press and release LOAD switch - Ready lamp goes out drive cycles down approx 45 sec. LOAD lamp illuminates.

12) Remove cartridge.

13) Base Address: 774400

14) Vector Address: 160 BR:5

15) Controller: RL11: M7762: Hex HT SPC.

Table 8-1 RL11/RL01 Diagnostics

Name	Description
CZRLAB0	Controller Test #1
CZRLBB0	Controller Test #2
CZRLCB0	Drive Test #1
CZRLDB0	Drive Test #2
CZRLEB0	Performance Exerciser
CZRLFB0	Compatibility Test

Table 8-2 RL11/RL02 Diagnostics

Name	Description
CZRLGA0	Controller Test #1
CZRLHA0	Controller Test #2
CZRLIA0	Drive Test #1
CZRLJA0	Drive Test #2
CZRLKA0	Performance Exerciser
CZRLLA0	Compatibility Test
CZRLMA0	Bad Sector File Utility

1.1 GENERAL DESCRIPTION

The RL01/RL02 Disk Drive is a random access mass storage device. Both drives utilize a removable, single platter top-loading disk cartridge. The RL01K cartridge provides five million bytes of storage, and the RL02K cartridge will hold ten million bytes. Up to four RL01 or RL02 Disk Drives may be used per controller to provide up to 40 million bytes of storage for PDP-8, PDP-11, and LSI-11 computer system applications.

The RL01/RL02 Disk Drive (Figure 1-1) is mounted on slides and is 26.6 cm (10.5 in) high, 63.5 cm (25 in) deep (compatible in width to a 19 inch RETMA rack) and weighs 34 kg (75 lbs).

Operating controls and indicators plus a removable air filter are located at the front of the drive. Access to the cartridge is provided by a lift-up cover incorporating a safety interlock. All servicing can be achieved from the top of the drive or front or rear of the corporate cabinet.

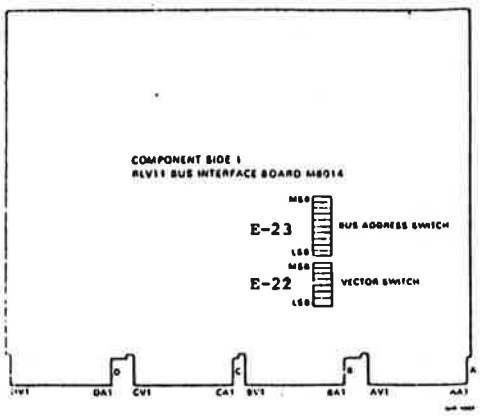
1.1.1 Servo-In-Data Concept

Key to the performance of the RL01/RL02 is the servo-in-data concept. The concept allows the derivation of head positioning and track counting information from pulses imbedded within the data track. Each read/write head seeking to a desired track becomes its own servo transducer. Data tracks could conceivably be located within a band anywhere on the recordable disk surface as long asthe positioner does not run out of travel limits. Since the heads seek and center on data tracks, environmental problems related to mechanical drift and tolerances become practically nonexistent. Precise head alignment requiring the use of special fixtures is unnecessary.

1.1.2 Storage Medium

The RL01K or RL02K Disk Cartridge is a modified 5440 type removable, top-loading, single platter cartridge with 256 discrete data tracks on each of the two recording surfaces. The cartridge armature plate contains 40 sector slots, defining 40 sectors per track. Servo information (servo-in-data) from which sector and track determinations are made is prerecorded on the cartridge at the factory and cannot be reformatted in the field. Bad sector information is contained on the last data track.

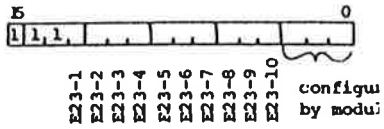
RL01K and RL02K cartridges are intended as a means of data interchange between computer systems. Data written on one RL01 Disk Drive will be readable on any other RL01 drive, and the same is true for any two RL02 drives, provided that both drives have been properly maintained and that the computer systems and controllers are compatible with respect to word length. Note, however, that an RL01K cartridge cannot be used on an RL02 drive, nor can an RL02K cartridge be used on an RL01 drive. While either cartridge will physically fit into either drive, the results of using the wrong cartridge are unpredictable. The cartridge are color keyed and labeled to help prevent incorrect use.



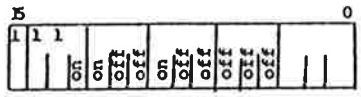
Note: Rocker switch positions are defined by depressing the desired side, not by the red line on the opposite side of the rocker.

0 = off
1 = on

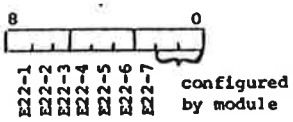
1. Address Selection



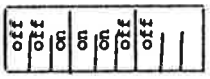
Factory configuration: 174400



2. Vector Selection

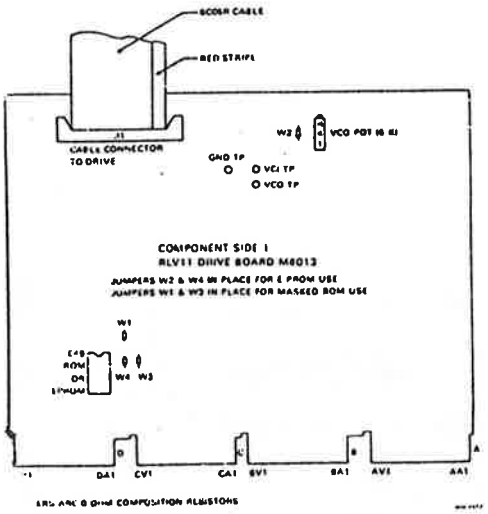


Factory configuration: 160

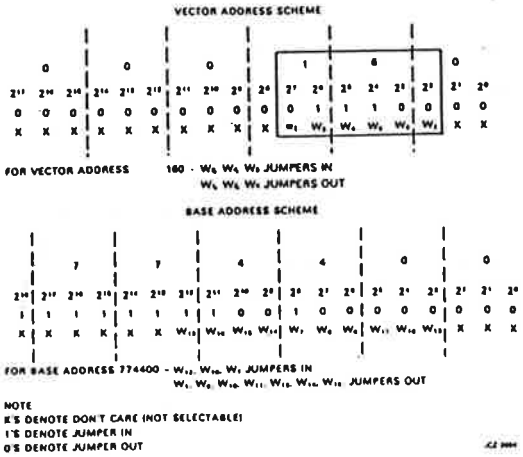


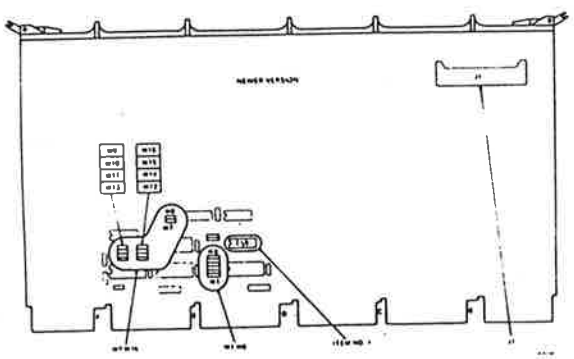
3. Miscellaneous Jumpers

W1 through W4 factory configured-do not change.



RL11 Configuration





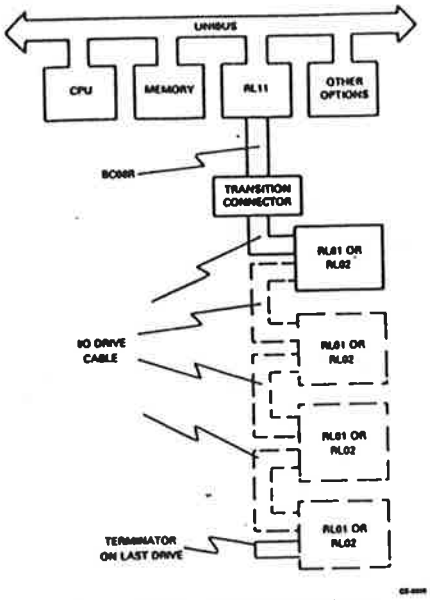
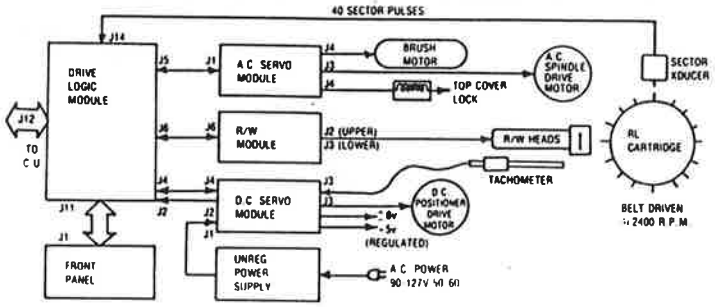


Figure 1-1 RL11-Based RL01/RL02 Disk Subsystem



RL01 MODULE FUNCTIONS

REGIONAL/AREA SPARES KITS RL SYSTEMS'

	RL01	RL02
R/W AMP	28419	33824 -
FRONT PANEL	28420	——
AC SERVO	28421	——
DC SERVO	28422	33825
DLM	28423	33826 - 45032 (Revl)
POSITIONER ASSY	28437	——
CABLE ASSY	28524	——
LAMP IND	24247	——
HEAD AUP	28425	33748 -
HEAD ADW	28426	33749
ABSOLUTE FILTER	28428	——
DISC PACK	6337	33667
FILTER AIR	28427	——

RKO6: 14.8MB

RKO7: 28MB

1) Switch on mains Cct Breaker on rear of Drive

2) Wait for STOP/RUN Lamp to illuminate

3) Press Cover release latch and raise cover

4) Insert cartridge, close cover

5) Press RUN/STOP switch ensure Lamp extinguishes

6) Wait for READY Lamp to illuminate

7) Boot device via consol emulator DM(CR) or toggle in Bootstrap

8) Do NOT remove system power while heads are loaded

9) Press and release RUN/STOP switch

10) READY Lamp extinguishes

11) Drive cycle's Down

12) RUN/STOP Lamp illuminates

13) Remove cartridge

14) Base Address : 777440 - (16)

15) Vector Address : 210 BR: 5

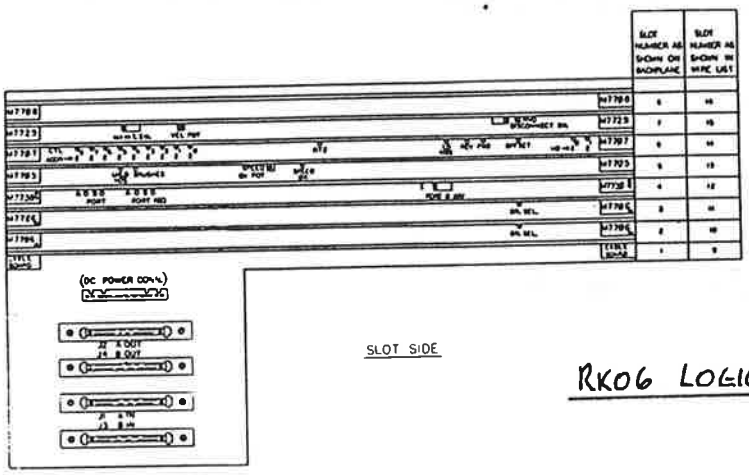
16) RK611 controller uses a 9 slot dedicated backplane M7900, 01, 02, 03, 04.

The RK06 uses a cartridge with two disk platters. Three of the four disk surfaces are used for data storage.

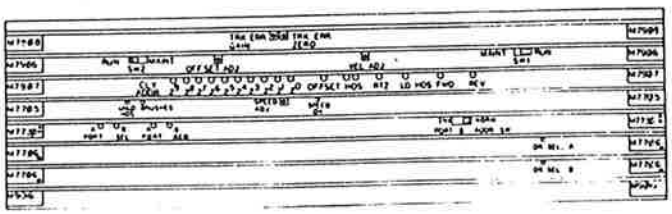
The fourth surface is a dedicated SERVO SURFACE, which is prerecorded at the time of manufacture with a repetitive pattern of TRIBITS. The servo surface is configured for 411 tracks on RK06 and all the servo tracks have the same number of tribits (6720).

The tribit output is used to do the following:-

1 Keep the heads on track.
2 Count the track crossings.
3 Produce Index and Sector information.
4 Produce the Write Clock.



RK06 LOGIC CAGE



RK07 LOGIC CAGE

RK611 DISK CONTROLLER

The RK611 consists of 5 Hex modules as follows:-

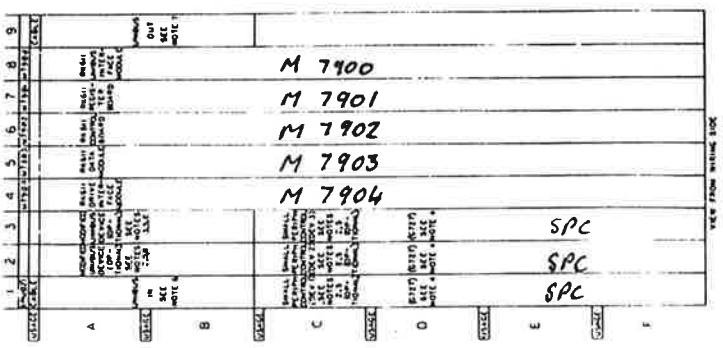
M 7900	Unibus Interface	UB	BIN - 28490
M 7901	Register Board	RG	28498
M 7902	Control Board	CN	28499
M 7903	Data Module	DA	28500
M 7904	Drive Interface	DR	28501

There are Dual in-line switches on the M7900 board for device and vector address selection. The only adjustment is R72 on DR1, which controls the frequency of a phase-locked oscillator.

The Controller contains 16 Unibus-addressable registers, one of which is not used.

The main functions of the Controller are:-

1 To interpret and execute Drive Commands.
2 To interpret and route Status information from the Drives to the Unibus.
3 To provide Status information relating to overall Subsystem operation.
4 To control the Data flow between Drives and Unibus.
5 To perform Data encoding and decoding.
6 To perform Error detection and correction.

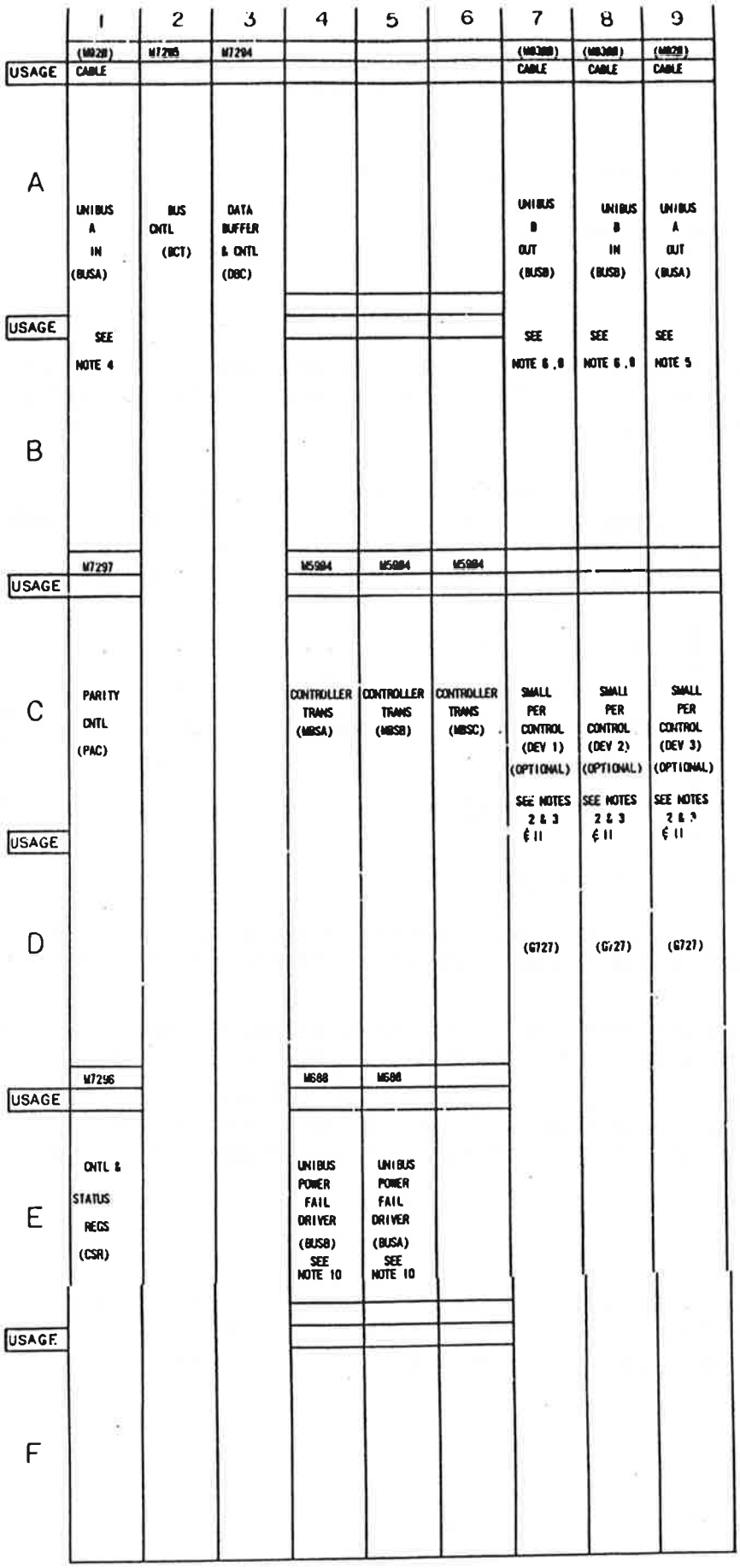


RK 611

RK06/7 DIAGNOSTICS

Program	Function
MAINDEC-11-DZR6A RK611 Diskless Controller Diagnostic Part 1	Reads and writes every RK611 register Tests the interrupt mechanism Tests the SILO loading logic. (Note: No drive is required for the execution of this program.)
MAINDEC-11-DZR6B RK611 Diskless Controller Diagnostic Part 2	Tests the loading of drive bus messages by executing Class A commands. Some Part 1 tests execute commands that are partially maintenance mode and partially at normal speed in order to "fool" the controller and force errors (no drive is required).
MAINDEC-11-DZR6C RK611 Diskless Controller Diagnostic Part 3	Tests the loading of the drive bus message shift register for Class B commands. Tests index and sector pulse detection. Tests SILO and NPR transfers from memory in 16- and 18-bit mode. Tests nonexistent memory and Unibus parity error detection. Tests Read and Write MFM loopback. Tests Class B instruction errors (no drive is required).
MAINDEC-11-DZR6D RK611 Diskless Controller Diagnostic Part 4	Tests loading of drive bus message shift registers for Class C commands. Tests header generation for search operations. Tests write data NPR transfers to SILO. Tests header recognition. Tests cylinder, track, and sector increment after successful header search. Tests detection of all header-type errors. Tests ECC generation and writing. Tests partial sector write (zero fill). Tests 18-bit format ECC generation and data write (no drive is required).
MAINDEC-11-DZR6E RK611 Diskless Controller Diagnostic Part 5	Tests multisector data transfers Tests midtransfer seeks. Tests cylinder overflow checking. Tests NPR transfers to memory. Tests ECC error detection and correction in 16- and 18-bit modes. Tests write check in both 16- and 18-bit modes and forces
MAINDEC-11-DZR6G Unibus RK06-RK07 Dual Port Drive Diagnostic (available Q4, FY78)	Tests write check errors (no drive is required). Ensures that port request, port seize, and timeout function correctly. Ensures that the release function operates correctly. Ensures that the timer inhibiting logic operates correctly. Ensures that data transfers function correctly through both ports.
MAINDEC-11-DZR6H Unibus RK06-RK07 Drive Diagnostic Part 1	Ensures that the drive can perform all static and cycle-up tests. Ensures that the drive can write and read headers in both 20- and 22-sector formats. (ie. it formats two pack) Ensures that the disk can perform seek operations by doing several seek patterns. Checks error-detection logic by software error forcing.
MAINDEC-11-DZR6I Unibus RK06-RK07 Drive Diagnostic, Part 2	Ensures that the disk is capable of performing read and write data operations in both 20- and 22-sector formats. Performs worst case patterns, spiral writing and reading, and all offset operations. No it doesn't! (Reports unloading and loading times.)
MAINDEC-11-DZR6J Unibus RK06-RK07 Drive Diagnostic, Part 3	Ensures that the disk is capable of performing all operator intervention functions properly. Checks error-detection logic by manual and by software forcing of errors.
MAINDEC-11-DZR6K RK611 Functional Controller Diagnostic	Tests those areas in the controller that cannot be tested in a diskless environment. Tests those areas of the drive that cannot be tested until controller operation in a diagnostic or maintenance mode has been tested.
MAINDEC-11-DZR6L RK06K-RK07K Cartridge Formatter	Writes and verifies header and data information on an RK06K or RK07K disk pack at all possible disk pack addresses. Uses the Bad Sector File to: (1) report the serial number of the cartridge being formatted, (2) determine whether the cartridge is an alignment cartridge, and abort the program if it is, and (3) identify the sectors that are to be marked "bad."

Program	Function
MAINDEC-11-DZR6M RK611/RK06-RK611/RK07 Subsystem Verification, Part 1	Provides a functional shakedown of the entire subsystem, including the Unibus interface and access to main memory. Employs worst-case situations involving mechanical positioning, disk addressing, and data transfer. Measures drive operational timing. Provides numerous options that may be specified by the user. Reports errors as they occur.
MAINDEC-11-DZR6N RK611/RK06-RK611/RK07 Subsystem Verification, Part 2	Continues functional shakedown provided by Part 1. Employs worst-case situations involving head offsetting, memory addressing and data transfer, Unibus cycle contention, and multiple-drive operations. Provides RK06 or RK07 head-alignment aid. Provides numerous options that may be specified by the user.
MAINDEC-11-DZR6P RK611/RK06-RK611/RK07 Performance Exerciser	Exercises in a random overlapped routine from one to eight RK06 or RK07 Drives connected to a common Unibus controller in a dedicated stand-alone mode. Generates read, write, and write check commands. Reports system errors upon occurrence. Maintains performance statistics on each drive.
MAINDEC-11-DZR6Q RK06-RK07 Drive Compatibility	Verifies the capability of each drive to write data that can be successfully read by all other drives of the same type and to completely overwrite data written by all other drives. Detects: (1) head misalignment, (2) positioner lateral misalignment, (3) spindle cartridge interface runout, (4) improper levels of write current, and (5) incorrect addressing of read/write heads. Prints summary of compatibility test results for each drive. Reports unexpected errors as they occur.
MAINDEC-11-DZR6R RK611/RK06-RK611/RK07 User Defined Test	Provides a capability for entering, editing, saving, recalling, and executing test programs designed by the user. Provides an interactive command set for use in entering, storing, retrieving, editing, and executing tests.



VIEW FROM WIRING SIDE

R.H 11

COMPUTER FIELD MAINTENANCE LIMITED

EQUIPMENT EVALUATION REPORT

AMPEX DM440 SERIES DISK DRIVE

There are 8 drives in the series which covers variants of fixed and removable platters, single and double density and front and top loaders. The following table shows the drive type relationship with the above variants:

	DM440	DM441	DM442	DM443	= FRONT LOAD
	DM445	DM446	DM447	DM448	= TOP LOAD
No. of Disks	1	2	1	2	
No. of Record Surfaces	2	4	2	4	
Tracks/Inch	100	100	200	200	
Capacity (MBytes)	2.5	5	5	10	
Max. No. of Cyls.	203	203	406	406	

In addition to the above there are variants of:

a) Voltage, 115 or 230 volts. Alteration of voltage involves not only the changes of transformer tappings, but a change of drive and blower motors, and also the auxiliary transformer.

b) Rotional speed, 1500 or 2400 RPM. The lower speed is not recommended as in the view of Ampex is more liable to contamination and hence breakdown.

c) Sectors. There can be 1, 8, 12, 14, 16, 20, 24 or 32 Sectors/Track. Note that any change to a different number of Sectors/Track for the removable disk would involve a rejumpering of the logic plus a change of the fixed disk sector wheel.

GENERAL DESCRIPTION

The drives are all similar in construction with the obvious exception of the top and front loading assemblies. They can be 19" rack mounted or used on a table and consist of the following sub-assemblies which can be individually removed from the drive:

1 Linear Motor Head Positioner Assy.

2 Rotational Drive and Cartridge Loading System

3 Electronic Module. 4 PCB's and Motherboard

4 Operator Control Panel

5 Internal Power Supply. (inc. 1 Reg. PCB.)

The drive is very similar in its technology vintage to the DEC RK03 using SSI (mainly 7400 Series) and should not prove to be a difficult drive to service.

GENERAL DESCRIPTION (Continued)

The AC drive motor is speed controlled to within +/-2% using the sector pick up.

The positioning assy. uses a photo-optical system that provides position and direction information to the electronics controlling the Linear Motor.

In addition to the high accuracy of the positioning, thermistors electrically compensate for dimensional changes caused by operational and environmental changes.

INTERFACE OPTIONS

The DM44X has obviously been designed to try to capture a large slice of the market as its options show.

Appendix C of the manual list and tables 25 I/O configurations for use of different controller manufacturers.

Drives leave the factory labelled on the drive exterior and on all PCB's with the I/O type for which it is strapped and any changes merit a change of these labels to avoid confusion.

MEDIA

Uses industry standard cartridges. IBM 5440 Top Load, IBM 2315 Front Load.

MTBF

Stated as >5000 hours, but some CFM experience possibly shows this as too high. Other contacts hint at 6 to 12 months.

Failures are linked very strongly to enviornment. Indeed, the Ampex Instructor stressed repeatedly the importance of regular filter changing and Manchester are now changing at least 1 drive's filters every 3 months. See MAINTENANCE.

DOCUMENTATION

All required documents are in the Maintenance Manual and include Flows, Descriptions, Maintenance Procedures and Schematics.

However, make sure that the manual is Revision B (August 1980) or later, as this version is greatly enhanced. Copies of this exist at MAD or LEE.

TRAINING

At present no CFM courses are planned, but a good course is available at Ampex, Reading for 1 week. This course gives hands on experience and costs aprroximately £300 to £400 depending on numbers.

MAINTENANCE

The manual recommends a 2 monthly cleaning and inspection visit with a 12 monthly air filter change and head alignment check.

MAINTENANCE (Continued)

I recommend a 3 month/6 month schedule minimum. This would tie in better with normal CFM practice and the shorter filter working life should give enhanced reliability. 6 month frequency of filter change assumes normal computer room environment. Filters may have to be changed at 3 month intervals and indeed at one 'Hoskyns' site it has been found necessary to change filters on a monthly basis.

It is important that Site Surveys reveal an initial chargeable filter change before it is too late.

Also, inferior environment should warrant an appropriate loading of the maintenance price, to reflect more frequent change of filter, etc.

Tools:

1 CE Packs Standard

2 PCB Extender (Approx. £70) Ampex (GB) Part No. 999DYN-047

3 Cleaning Wand. (Necessary for fixed Disks)

4 Disk Exerciser. (Seeks Only) Ampex (GB) Part No. 999DYN-051

5 Suitcase Tester. (Seek/Write/Read/Compare)

REPAIRS

Whilst I expect that most repairs should be handled either on site or at least at the local Service Centre, MAD is the designated repair centre for this drive.

Local purchase of an extender and a disk exerciser should enable local repair of 90% of faults.

I will look into the possibility of CFM manufacture of an exerciser, but extenders are a must at local level.

NOTE: Before sending in a PCB to MAD, please make sure that all adjustments have been checked ** in your drive **, e.g. a good A3 PCB (Servo) can be apparently U/S in another drive. See 1983 Tech. Tips regarding this drive.

SPARES

There is an existing Spares List done by Spares Engineering. This will be checked now that we have some knowledge of the equipment and updated as found necessary.

Ampex (GB) Ltd use a different set of numbers from those in the manual. To obtain spares quickly use this list as anything not easily converted to their system is passed on to the United States with its attendant delays.

SYSTIME CE SET UP

Note that Ampex drives on Systime systems vary as follows:

(Double Density)	CE Set Up	Track 200	(Industry Standard 210)
	Check	Track 210	(Industry Standard 220)
	Index to Burst	Track 190	(Industry Standard 200)

SECTION 7

TAPES

DEVICE/CONTROLLER			MODULE	DESCRIPTION	BOOT MNEMONIC
TS11	MS11		M7982	SPC SLOT	MS
TU10	TMB11		VARIOUS	DEDICATED B/P	MT
TS03	TMB11		"		MT
DIGIDATA 30		MAXI MINI	FORMATTER		MT
DIGIDATA 40					MT
TU58	DL11		M7856	SPC	DD

MAGNETIC TAPE SYSTEM

FORMATS

NRZI:

In this format a 'one' is written as a flux reversal on the tape, a 'zero' is ignored.

Phase Encoded:

In this format a 'one' is represented by a flux change from erase to the opposite polarity. A zero is represented by a change to erase from a opposite polarity. This necessitates the use of a reset bit, and effectively doubles the frequency for all ones or all zero bit patterns.

Group Coded Recording:

In this format four bits of data are recoded in to 5 bits of data. This enables the use of patterns with no more than 2 bit zero data together.

DENSITY

7 Track : 200, 556 or 800 BPI NRZI

9 Track : 800 BPI NK2J, 1600, 3200 BPI P.E.
6450 BPI GCR

TU10	7 Track	200, 556, 800 BPI
	9 Track	800 BPI
Speed	45 IPS	
Buffering	Vacumn	
Mnemonic	MT	
TS03	9 Track	800 BPI
	12.5 ISP	
	ARM	
	MT	
TS11	9 Track	1600 BPI
	45IPS	
	ARM	
	MS	

DIGI DATA — 7 Track/9 Track

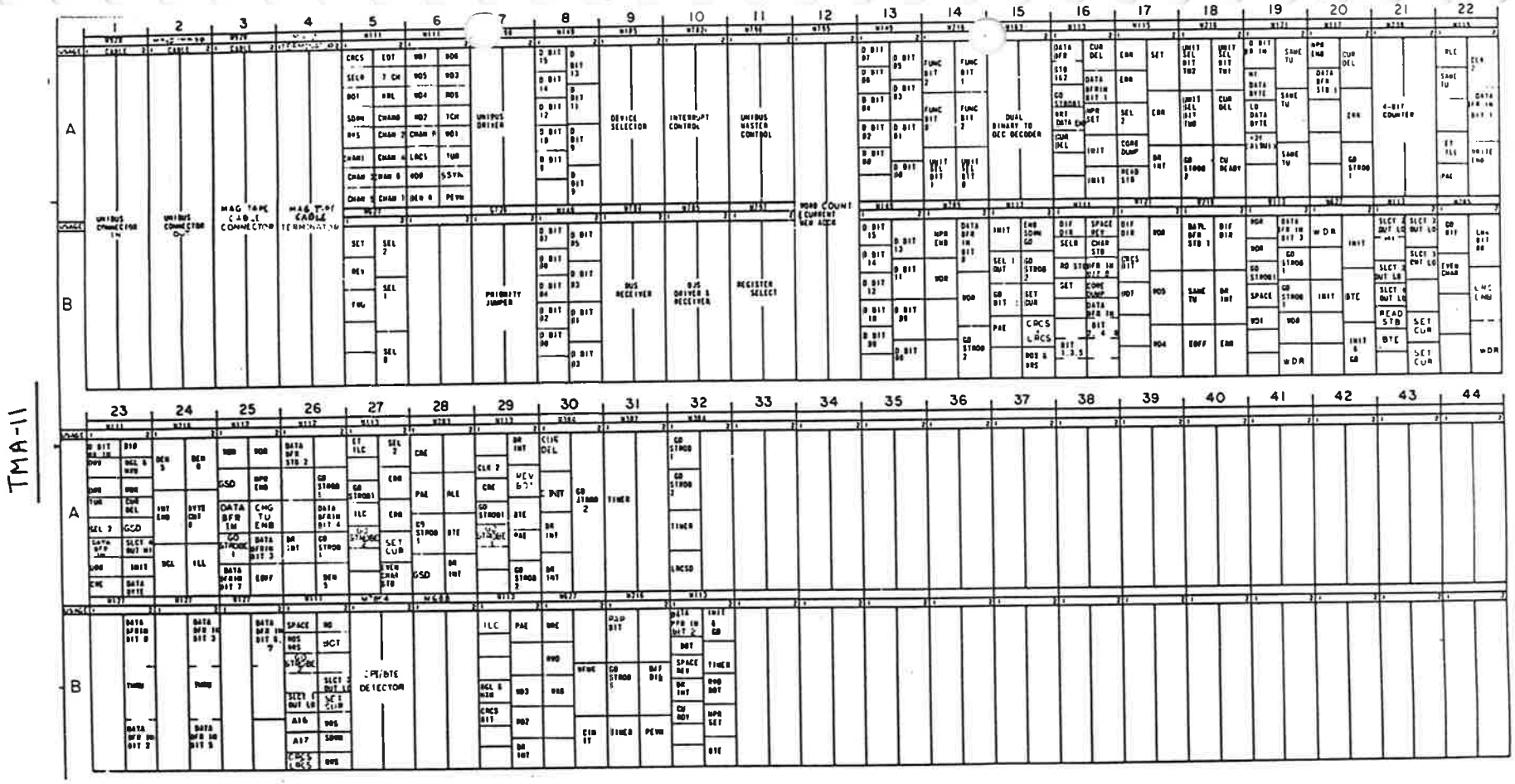
XXYZ

XX = REEL SIZE	11 - 600	MINI
	16 - 1000	MIDI
	17 - 2400	MAXI
Y = SERIES	3 - 30	SERIES
	4 - 40	SERIES
Z = No of Tracks	7 - 7	TRACK
	9 - 9	TRACK

MAGNETIC TAPE TRANSPORTS

	TU58	TS11	TE16	TU77	TU78
READ/WRITE SPEED	30 in/s	45 in/s	45 in/s	125 in/s	125 in/s
RECORDING DENSITY	800 b/in	1600 b/in	800/1600 b/in	800/1600 b/in	1600/6250 b/in
TAPE THREADING	N/A	MANUAL	MANUAL	AUTOMATIC	AUTOMATIC
REWIND TIME	N/A	2 min PER REEL	3.7 min PER REEL	65 s PER REEL	65 s PER REEL
OFF-LINE DIAGNOSTICS	N/A	YES	NO	NO	YES
MEDIA TYPE	CASSETTE CARTRIDGE	½ in TAPE REEL-TO-REEL	½ in TAPE REEL-TO-REEL	½ in TAPE REEL-TO-REEL	½ in TAPE REEL-TO-REEL
NO. OF TRACKS	2	9	9	9	9
STORAGE CAPACITY (8 KB BLOCKS)	262 KB PER CARTRIDGE	40 MB PER REEL	40 MB PER REEL	40 MB PER REEL	145 MB PER REEL
PEAK TRANSFER SPEED	3.7 KB/s	72 KB/s	72 KB/s	200 KB/s	780 KB/s
TAPE BUFFERING	N/A	TENSION ARM	VACUUM COLUMN	VACUUM COLUMN	VACUUM COLUMN
TRANSPORTS PER FORMATTER	2 (only one works at a time)	1	8	4	4
		MS-11			
Controller	DL11	M7982	RH11	RH11	RH11

	TA11	TC11/TU56	TS03	TM11/TU10	TU16
READ/WRITE SPEED	9.6 In/Sec	97 IPS	12.5 IPS	45 IPS	45 IPS
RECORDING DENSITY	350 - 700 P.E	350 BPI	800 BPI	200/556/800	800/1600
REWIND TIME	20 Sec		1 Minute	350 IPS 3 Minutes	150 IPS 3 Minutes
NO. OF TRACKS	1	10	9	7/9	9
STORAGE CAPACITY	90 KB	295 KB	5 MB	20 MB	32 MB
TAPE BUFFERING	Reel To Reel	Reel	Arm	Vacumn	Vacumn
PEAK TRANSFER SPEED	560 B/S	10 KB/S	10 KB/S	36 KB/S	72 KB/S
Controller	-	TC-11	TMB-11	TMB-11	TJU16



TM811

				SLOT
MAG TAPE CABLE	WORD COUNT & CURRENT MEMORY ADDRESS M795		UNIBUS OUT (BCIIA)	4
TERMINATOR M930	ADDRESS SELECTOR M105	UNIBUS MASTER CONTROL M796	INTERUPT CONTROL M7821	3
UNIBUS REGISTER M7912				2
TAPE DRIVE INTERFACE M7911			UNIBUS IN (BCIIA)	1
F	E	D	C	B A

OPERATING INSTRUCTIONS FOR DIGI-DATA M.T.U.

1. Ensure Unibus Connector Cable is fitted in place of M 930/9302.

2. Switch on Logic Package power before powering up 11/34 processor.

3. Press Power switch on MAGTAPE DRIVE UNIT. Green light adjacent should light.

4. Place magtape reel on lower supply reel hub on Magtape Drive Unit.

5. Follow tape threading diagram on Drive Unit.

6. Press Load button. Tape should move until it reaches begining of tape BOT mark and then stop.

7. Press ON-LINE buttom. Green lamp adjacent will light.

8. Green RING lamp will light to indicate that the tape is not write protected. To write protect reel remove write ring on reverse side of reel.

9. To unload tape press rewind button and wait until tape stops at BOT press rewind button again and tape will slowly un-thread.

10. Controller/Formatter cable is inserted into a Unibus Out slot only: Normally last slot on Backplane.

    NB A terminator M930/9302 must be installed in the Control Unit.

11. Base Address 772520

12. Vector Address 224

13. Boot Device from Consol Emulator using M.T. <CR>

RUNNING INSTRUCTIONS FOR TS11

1. Switch Power on.
2. Ensure UOK Light illuminated.
3. Open door and load tape as per Threading Diagram.
4. Close door.
5. Press LOD button.
6. TS11 should now load tape. LOD should illuminate and BOT should illuminate.
7. Press ONL. TS11 should now be online.
8. WLK will illuminate if tape is write protected.

TSBA 772522

TSSR 772524

VECTOR 224

TS11 Controller: M7982 : Any S.P.C. Slot

Remove write Protect Ring (on tape Reel) to write protect MEDIA.

RED STRIPE at top.

Boot Device from consol emulator using M.S. ⟨CR⟩

Table 2-2 Address and Vector Examples

ADDRESS						
7	7	2	5	2	0	
x x x	x x 1	0	1 0 1	0 1 0 1	0 0	x x
	E34	E90				
x x x	x x 1	1 10 9	8 7 6	5 4	3 2	x x
x x x	x x off	on off on	off on off	on off	on	on x x

on = 0; off = 1

VECTOR						
0	0	0	2	2	4	
x x x	x x x	x x x	0 1 0 0	1 0	1	x x
			E34			
x x x	x x x	x x x	8 7 6	5 4	3 2	x x
x x x	x x x	x x x	on off on	on off on	off	x x

on = 0; off = 1

5. Cut CA1 to CB1 (NPG) jumper on the SPC backplane slot.
6. Insert the M7982 module into any available SPC slot and connect the serial bus interface cable attached (TS11-J1 to motherboard J4).

   NOTE
   The M7982 LED lights up if the interface cable is reversed.

7. Verify correct voltage and frequency at the rear of the transport.

   NOTE
   When 50 Hz power is used, both switches on the G158 board must be in the open or off position. (At 60 Hz both must be closed or on.) Also, verify that the ac input box (TS11 Power Supply) is correct. It is necessary to check the tension arm adjustment when changing from 60 Hz to 50 Hz power.

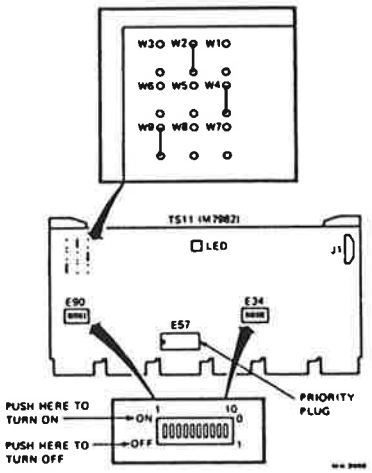


Figure 2-1 M7982 Interface Module

8. Power up the transport and verify all voltages. (Refer to Paragraph 5.1).
9. Place the transport in maintenance mode and view the PC lights. Check for errors.
10. Load a tape (tape will not be positioned at BOT).
11. Run internal diagnostics, the control logic test, then the data reliability test. (Test 47 fails in auto-sequence mode if the M7982 is not powered up.)

1) Ensure DL 11 is attached and correctly SET. Switch on Mains Drive.

2) Load Cartridge (Drive Ø Left Hand Side)

3) Boot device via consol emulator D.D. ⟨CR⟩ , or a Toggle in Bootstrap routine.

4) There appears to be a bug with the majority of TU 58 Systems, in that the CPU will initially run and then halt at Location 554.

5) In this event Load Address 574 and press Control/Start. The device will then boot normally.

6) DL 11 W Switch Setting

   a) Base Address 776500
   b) Vector " 300
   c) Baud Rate 9600
   d) Parity None

7) Break must be enabled.

8) LTC must be Disabled.

9) Error bits must be Disabled.

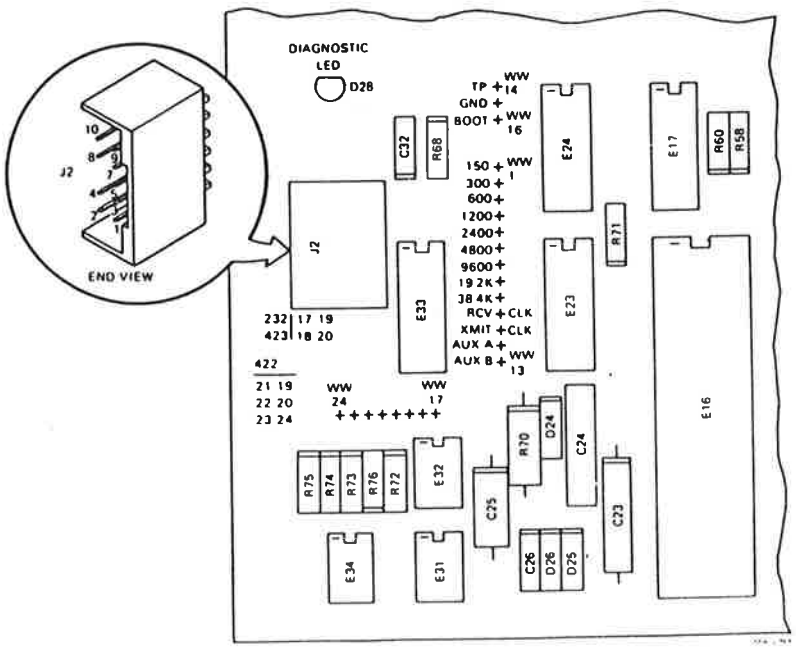


Figure 13 Interface Selection Jumper Pin Locations

SECTION 8

LSI/UNIBUS SIGNAL CROSS REFERENCE

UNIBUS	Q BUS
ADD (18)	BDAL (18)
DATA (16)	
NPR	BDMR
NPG	BDMG
BR	BIRQ
BG	BIAK
HALT REQ	BHALT - ODT
HALT GRANT	-
DC LO	BDC OK
AC LO	BPOK
1WNT	BINIT
SACK	BSACK
MSYNC	B SYNC L
SSYNC	B REPLY L
BBSY	B SYNC - held
CO C1	
DATO	BDOUT
DAT1	BDIN
DATOB	BWTBT
DATIP	-
	BBS7 (I/O PAGE) A16:17
	BREF MEMORY REFRESH
	BEVNT LINE TIME CLOCK IN

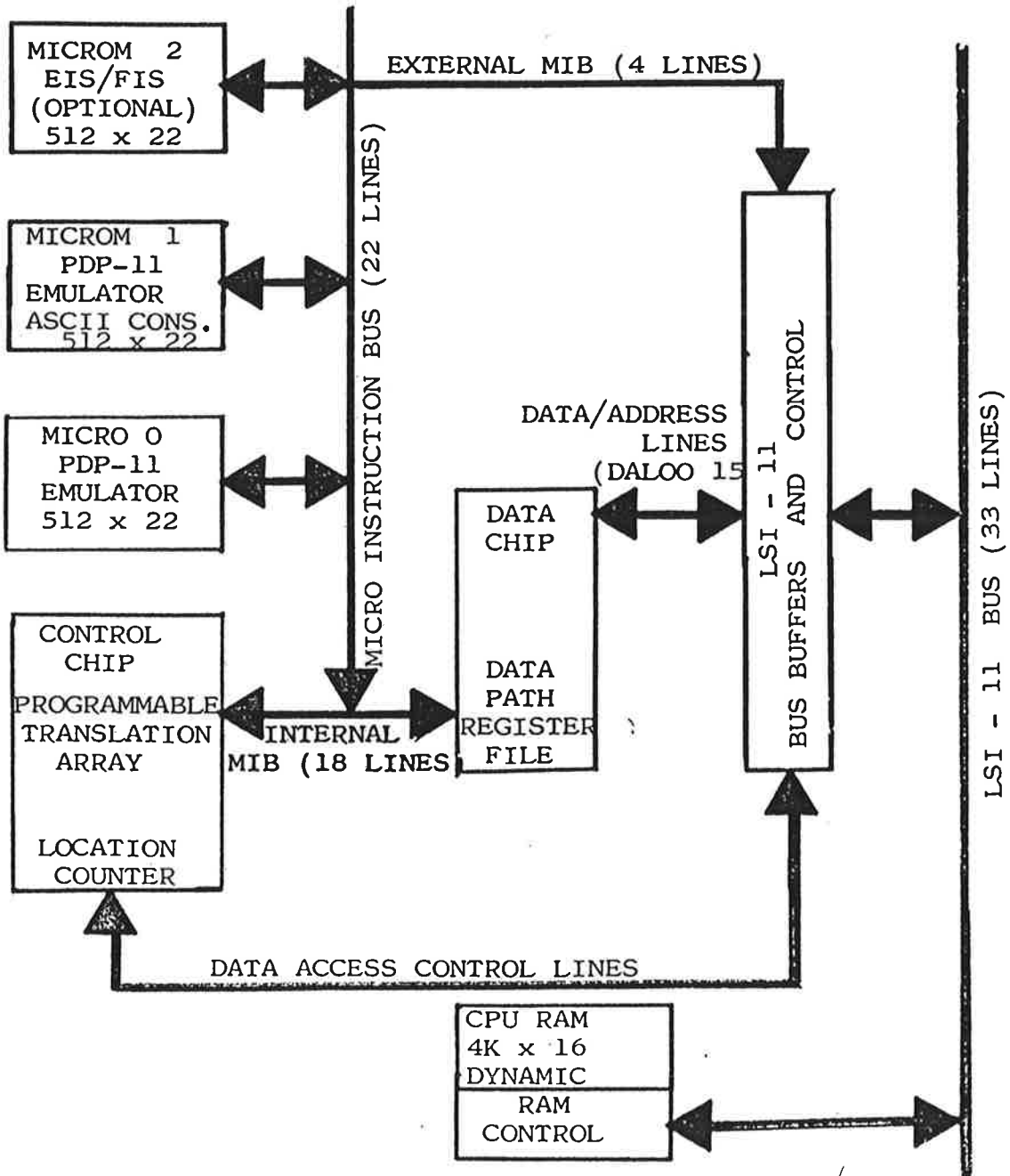
LSI-11 BUS

Bus data and control lines are bi-directional open collector lines that are asserted low.

THE BUS IS COMPOSED OF:-

16 Data/address lines.

20 control/synchronization signal lines.



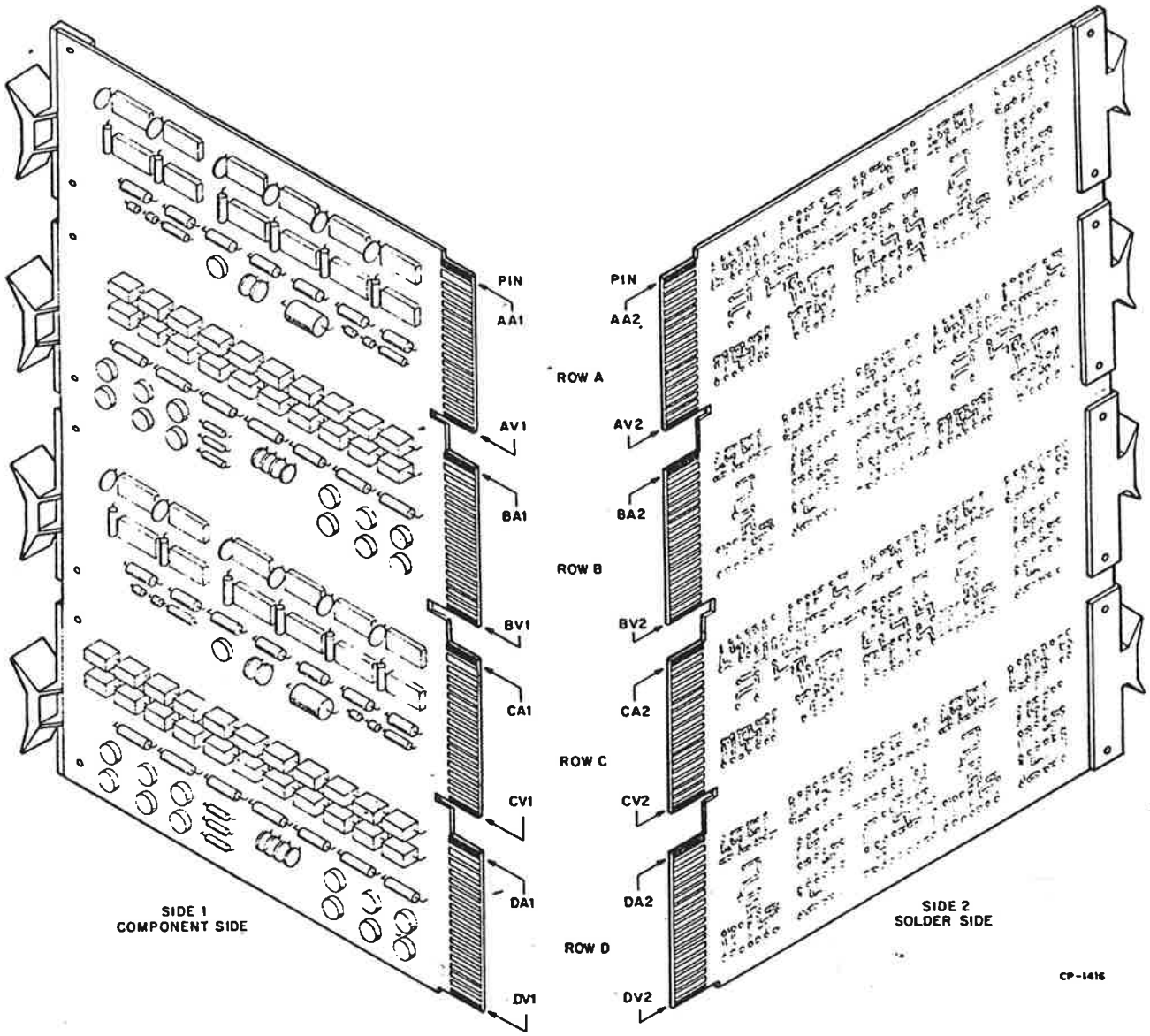
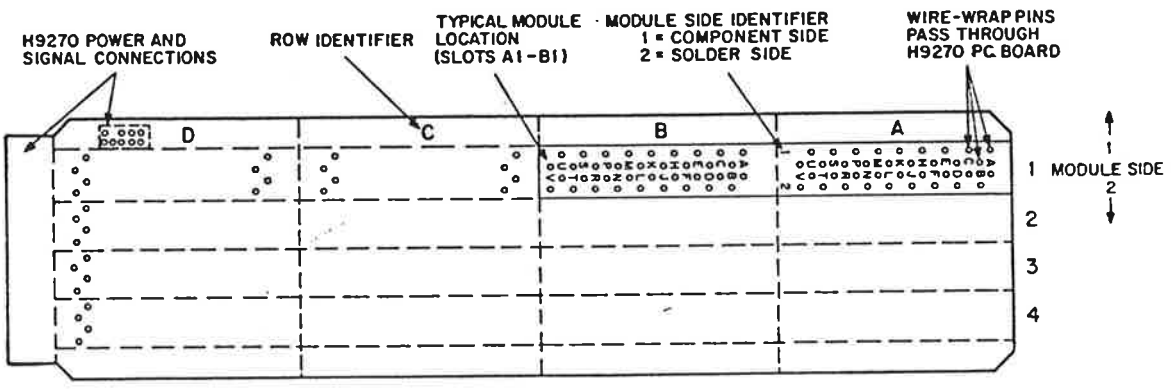


Figure 3-2 Quad Module Contact Finger Identification



LSI-11, PDP-11/03 Backplane Module Pin Identification

LSI BUS PROCESSORS

LSI-11

The LSI-11 processor was introduced in 1975 and was the forerunner of 16 bit architecture microcomputers.

The LSI-11 is capable of 32kw direct addressing incorporating ODT consol emulator routines and comes complete with 4KW on board memory - Quad height PCB.

Device Mnemonic	Module	Description	Bin
KD-11F	M7264	LSI-11 Processor + Ram	20719
KD-11F	M7264-YC	" " Less Ram	28049

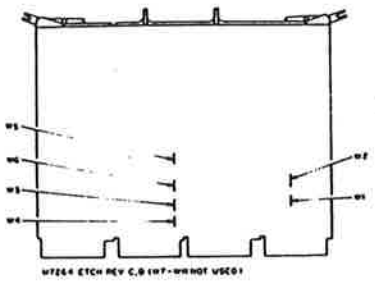
OPTIONS

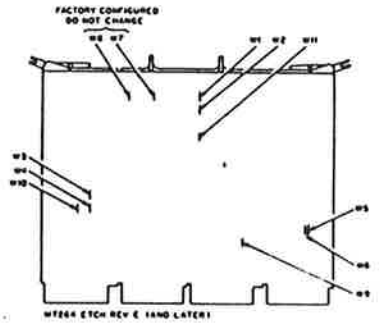
KEV-11 40 Pin Chip EIS/FIS

Table 15-1 LSI-11 Processor Module Factory-Installed Jumpers

	M7264		M7264-YA	
Jumper	Status	Function	Status	Function
W1	R	Resident memory bank 1 not selected	R	Resident memory bank 1 not selected
W2	I	Resident memory bank 0 selected	R	Resident memory bank 0 not selected
W3	R	Event line (LTC) interrupt enabled	R	Event line (LTC) interrupt enabled
W4	R	Processor-controlled memory refresh enabled	I	Processor-controlled memory refresh disabled
W5	R	Power-up mode	R	Power-up mode
W6	R	0 selected	R	0 selected
W7	—	Factory-configured bias voltage (do not change)	—	Factory-configured bias voltage (do not change)
W8	—		—	
W9	R	Enable reply from resident memory	I	Disable reply from resident memory
W10	R	Enable reply from resident memory during refresh	R	N/A
W11	I	Enable on-board memory select	R	Disable on-board memory select

Mode	W6	W5	Mode Selected
0	R	R	PC at 24 and PS at 26, or Halt mode
1	R	I	ODT microcode
2	I	R	PC at 173000 for user bootstrap
3	I	I	Special processor microcode (not implemented)





H9270

A	B	C	D
← PROCESSOR MODULE →			
OPTION 2		OPTION 1	
OPTION 3		OPTION 4	
OPTION 6		OPTION 5	

NOTE 1. Unused slots require backplane jumpers for BIAKI/O L, BDMGI/O L

DIAGNOSTICS

VKAA - CPU

VKAB - EIS

VKAC - FIS

VKAP - INT/TRAP

VKAE - DLV11

VKAF - DRV11

VKAH - 4 K SYSTEM TEST

LSI-11/2

Introduced 1977 based on the same chip set as LSI-11 but mounted on a dual height PCB. No on board memory, 32kw addressing.

4 Chips Basic: Control
Data Paths
Micro instruction Rom
Micro instruction Rom

KEV-11 Optional EIS + FIS

Device Mnemonic	Module	Description	Bin
KD11-HA	M7270	LSI-11/2 Processor	30653

OPTIONS

KEV-11 40 Pin Chip EIS + FIS

DDV11-B

A	B	C	D	E	F	
← PROCESSOR →						1
OPTION 2		OPTION 1				2
OPTION 3		OPTION 4				3
OPTION 6		OPTION 5				4
OPTION 7		OPTION 8				5
OPTION 10		OPTION 9				6
OPTION 11		OPTION 12				7
OPTION 14		OPTION 13				8
OPTION 15		OPTION 16				9

USER DEFINED SLOTS

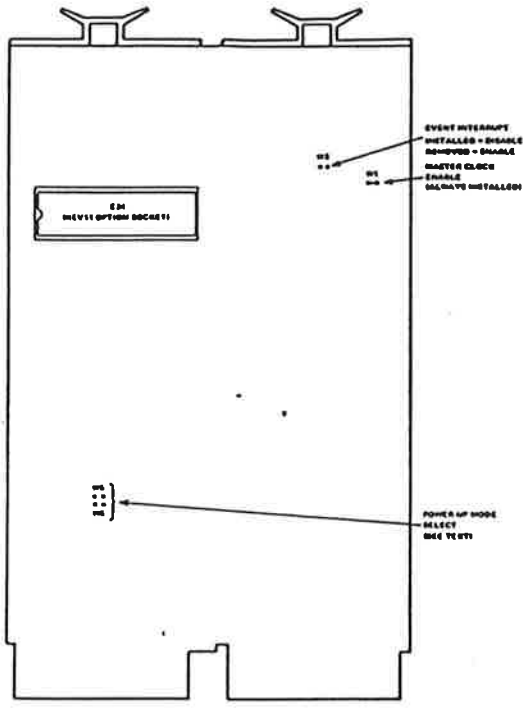


Figure 14-1 M7270 Processor Module Jumper Locations

DIAGNOSTICS

VKAA - CPU
VKAB - EIS
VKAC - FIS
VKAP - INT/TRAP
VKAE - DLV11
VKAF - DRV11
VKAH - 4 K SYSTEM TEST

Table 14-2 LSI-11/2 M7270 Processor Module Factory-Installed Jumpers

Jumper	Status	Function
W1	I	Master clock enable (always installed—do not remove)
W2	N/A	
W3	R	Event line (LTC) interrupt enabled
W4	N/A	
W5	R	Power-up mode 0 selected
W6	R	

NOTES
1. Do not change W1 on the LSI-11/2 M7270 module. It is always installed.

Table 14-3 Power-up Jumpers

Mode	W6	W5	Mode Selected
0	R	R	PC at 24 and PS at 26, or Halt mode
1	R	I	ODT microcode
2	I	R	PC at 173000 for user bootstrap
3	I	I	Special processor microcode (not implemented)

R = Jumper Removed; I = Jumper Installed.

LSI-1123

Introduced in 1979, Data Paths, Control and microinstructions now intergrated into a single 40 pin chip - 2.5 times faster than LSI-11. With the memory management chip option the 1123 is capable of addressing 128kw of memory, EIS standard.

In 1981 22 bit addressing capability was added to increase the address range up to 2mw. (CATCH 22: Software)

Mnemonic	Module	Description	Bin
KDF-11AA	8186 (Dual)	LSI11/23 Processor	34046

OPTIONS

KEF-11	40 Pin Chip	Memory Management
KEF-11	" " "	Floating Point
FPF-11	M8188 (Quad)	Floating Point

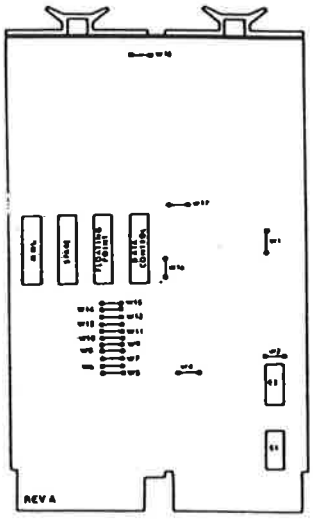


Figure 13-1 LSI-11/23 Jumper Locations (Rev. A)

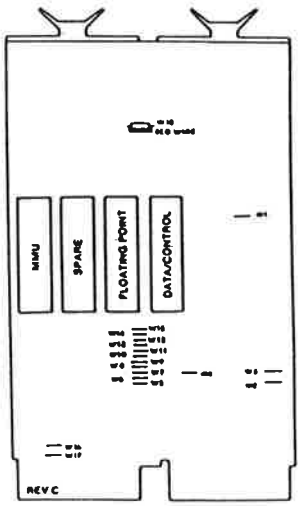


Figure 13-2 LSI-11/23 Jumper Locations (Rev. C)

Table 13-2 Jumper Configurations

Jumper	Name	In	Out
W1	Master clock	Enable internal master clock	Do not remove. Manufacturing use only
W2	Reserved for DIGITAL use	Factory-installed	Do not remove
W4	Event line enable	Disabled	Enabled
W5,W6	Power-up mode selector	See text	See text
W7	Halt/trap option	Trap to 10_8 on halt	Enter console ODT on halt
W8	Conventional bootstrap start address, enable if power-up mode 2 is selected	Power-up to bootstrap address 173000_8	Power-up to bootstrap address selected by jumpers W9-W15
W9-W15	User-selectable bootstrap starting address for power-up mode 2	See text	See text
W16	Reserved for DIGITAL use	Must be installed	Do not remove
W17	Reserved for DIGITAL use	Must be installed	Do not remove
W18	Wake-up Circuit	Disabled	Enabled

Mode	Name	W6*	W5*
0	PC@24, PS@26	R	R
1	Console ODT	R	I
2	Bootstrap	I	R
3	Extended microcode	I	I

*R = jumper removed, I = jumper installed

DIAGNOSTICS

JKDA - MEMORY MANAGEMENT

JKDB - CPU

JKDC
JKDD - FLOATING POINT

FALCON SBC 11/21

Single board computer, introduced in 1981 utilising the 16 bit micro T-11 processor. Direct addressing of 32KW of memory. The Falcon incorporates on board Ram (4kb) and Rom (32kb). 2 serial line units, plus a real time clock, there is an added availability of 24 parallel data lines (3 ports).

The micro T-11 was developed from the LSI-11 chip set and is aproximately twice as fast, but has a smaller instruction set than the 1123.

NB. T-11 cost is approx. £30 as opposed to 1123 @ £120

Mnemonic	Module	Description	Bin
KXT11-AA	M8063 (D)	Falcon SBC	-

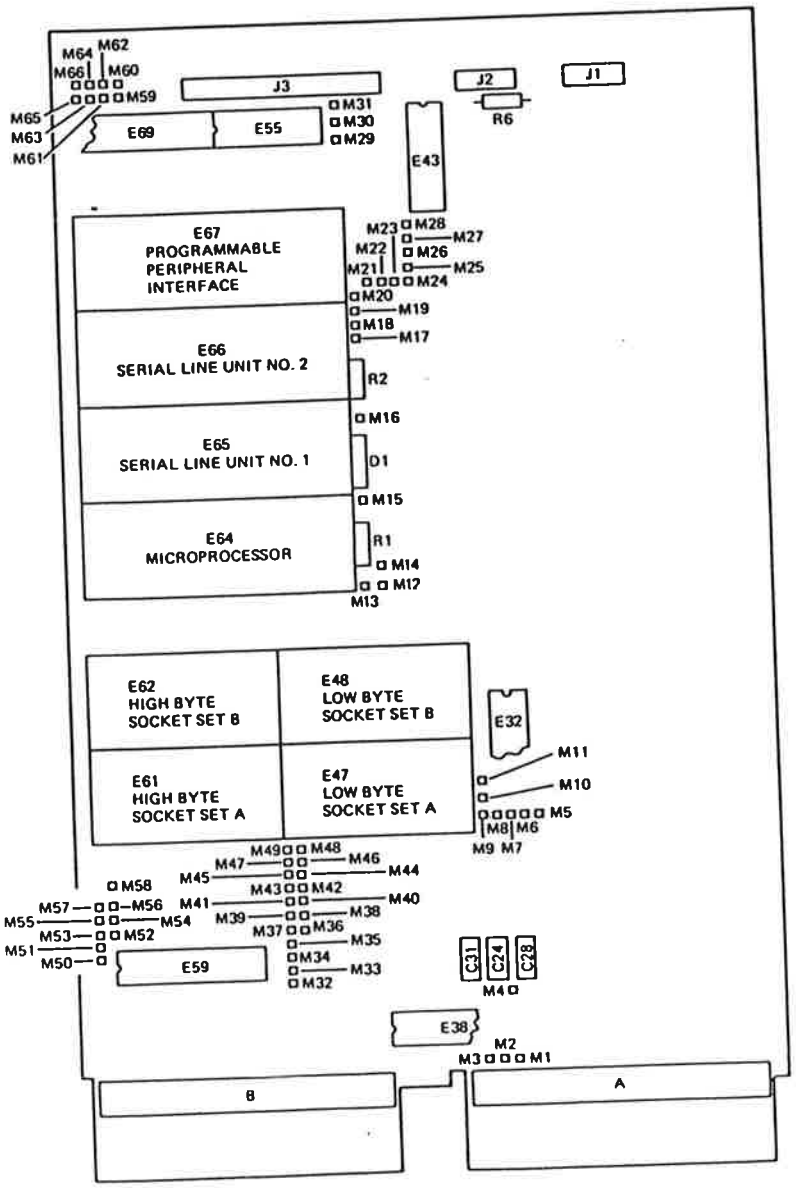


Figure 12-1 FALCON SBC-11/21 Module Map

1123 PLUS

The 1123 plus utilises the 1123 chip set, and incorporates 22 bit addressing (2mw) as standard. The 1123 plus incorporates on board bootstrap and diagnostic functions, LTC and 2 SLU's.

Mnemonic	Module	Description	Bin
KDF11-B	M8189	1123 plus processor	-
OPTIONS			
KEF-11	40 pin Chip	Floating Point	
	" " "	C.I.S.	

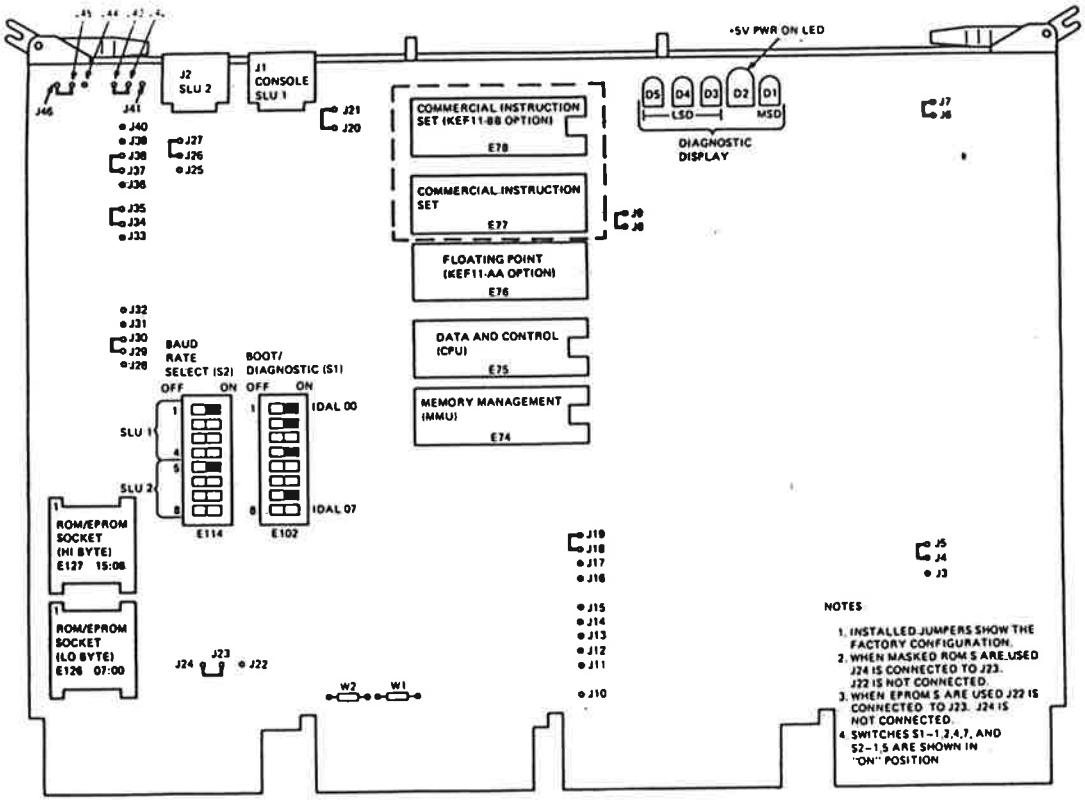


Figure 22-5 PDP-11/23-PLUS Jumper, Switch and Diagnostic Display Locations

VMSA?? : 22 bit memory Diagnostic

LSI-11 SYSTEM's

PDP1103	:	LSI-11 OR LSI-11 PROCESSOR	
PDP1103-L	:	LSI-11/2 PROCESSOR	
PDP1123	:	LSI-1123 PROCESSOR	
PDP11T03	:	LSI-11/2 PROCESSOR	RL01/2 DISC DRIVES
PDP11T23	:	LSI-1123 PROCESSOR	RL01/2 DISC DRIVES
PDP11V03	:	LSI-11/2 PROCESSOR	RX02 DISC DRIVES
PDP11V23	:	LSI-1123 PROCESSOR	RX02 DISC DRIVES
PDP1123 PLUS:		LSI-1123 PROCESSOR	RL02 DISC DRIVES

LSI-11 MEMORY

A) ROM MEMORY

Mnemonic	Module	Description	Bin
MRV11-AA	M7942 (D)	4k x 16 PROM Board	39402
MRV11-BA	M8021 (D)	4k x 16 EROM/256w RAM	39576
MRV11-C	M8048 (D)	32KW PROM/EPROM- Bootstrap Capability	-

B) RAM MEMORY

MSV11-B	M7994 (D)	4k x 16 RAM	28658
MSV11-CD	M7955-YD (Q)	16k x 16 PAM	28053
MSV11-DA	M8044-A	4k x 16 RAM	-
MSV11-DB	M8044-B	8k x 16 RAM	-
MSV11-DC	M8044-C	16k x 16 RAM	-
MSV11-DD	M8044-D	32k x 16 RAM	34045
MSV11-EA	M8045-A	4k x 18 (Parity)	-
MSV11-EB	M8045-B	8k x 16 (Parity)	-
MSV11-EC	M8045-C	16k x 18 (Parity)	-
MSV11-ED	M8045-D	32k x 18 (Parity)	-
MSV11-LF	M8059-FA	62k x 18	-
MSV11-LK	M8059-KA	128k x 18	-
MCV11-DC	M8631-	16kw CMOS Battery RAM	

MULTIFUNCTION MODULES

MXV11-AA	M8047-AA	4kw RAM,2 S.L.U's 4kw PROM/Boot	-
MXV11-AC	M8047-AC	16kw RAM	34047

SERIAL LINE UNITS

Mnemonic	Module	Description	Bin
DLV11	M7940	Asynchronous Serial Line Unit	20721
DLV11-E	M8017	S.L.U. with MODEM Control	38752
DLV11-F	M8028	No MODEM Control, Reader Run,19,200 Baud	28059
DLV11-J	M8043	4 x S.L.U's BELL103 EIA	28058
DLVAA-KA		EIA - 20MA Convertor	-
DRV11	M7891 (D)	Parallel Interface (GP)	35526
DRV11-B	M7950 (Q)	" " (DMA)	-
DRV11-J	M8049 (D)	4 Port Parallel I/O	-
DRV11-P	M7948 (Q)	Foundation Module	-
DUV11	M7951 (Q)	BELL 201 Synchrounous I/O	-
DZV11	M7957 (Q)	4 Channel Async Mux.	39046
DPV11	M8020 (D)	Synchronous I/O	-

LS1-11 DISC CONTROLLERS

MNEMONIC	DRIVE	MODULE	DESCRIPTION	BIN
RKV11-D	RK05	M7269	Disc controller	-
RLV11	RL01/2	M8013 M8014	Drive interface Bus interface	28054 28055
RLV12	RL01/2	M8061	Disc controller	-
RXV11	RX01	M7946	Floppy disc controller	20396
RXV211	RX01/2	M8029	Floppy disc controller	35007

Option Desig.	Module No(s).	Description	Power Requirements +5V ±5%	Power Requirements +12V ±3%	Bus Loads* AC(Max)	Bus Loads* DC	Size
AAV11-A	A6001	4-channel, 12-bit D/A converter	1.5 A	0.4 A	1.9	1	Quad
AAV11-C	A6006	4-channel, 12-bit D/A converter	2.0 A	–	0.9	1.0	Double
ADV11-A	A012	16-channel, 12-bit A/D converter	2.0 A	0.45 A	3.25	1	Quad
ADV11-C	A6000	16 single-ended or 8 differential A/D channels, 12-bit	1.5 A	–	1.3	1.0	Double
AXV11-C	A0026	Analog I/O board 16 single-ended analog input channels, 12-bits 2 D/A output, 12-bit channels	1.5 A	–	1.3	1.0	Double
BDV11	M8012	Bootstrap, terminator, diagnostic	1.6 A	0.07 A	2.0	1	Quad
DDV11-B		6 X 9 backplane			6.4	0	
DLV11	M7940	Asynchronous serial line interface	1.0 A	0.18 A	2.5	1	Double
DLV11-E	M8017	Asynchronous line interface	1.0 A	0.18 A	1.6	1	Double
DLV11-F	M8028	Asynchronous line interface	1.0 A	0.18 A	2.2	1	Double
DLV11-J	M8043	4 asynchronous serial interfaces	1.0 A	0.25 A	1	1	Double
DPV11	M8020	Synchronous serial line interface	1.2 A	0.30 A	1.0	1.0	Double
DRV11	M7941	Parallel line unit interface	0.9 A	–	1.4	1	Double
DRV11-B	M7950	DMA interface	1.9 A	–	3.3	1	Quad
DRV11-J	M8049	64-line parallel I/O	1.6 A	1.6 A	2.0	1	Double
DRV11-P	M7948	Foundation module	1.0 A +user logic	–	2.1	1	Quad
DUV11	M7951	Synchronous serial line interface	0.86 A	0.32 A	1.00	1	Quad
DZV11	M7957	Asynchronous line interface	1.15 A	0.39 A	3.95	1	Quad
FPF11	M8188	Floating point processor	5.5 A	–			Quad
H9270		4 X 4 backplane			5.1	0	
H9273		4 X 9 backplane			2.6	0	
H9275-A		4 X 9 backplane	–	–	10.0	0	
H9281A		2 X 4 backplane			1.3	0	
H9276		4 X 9 backplane			2.6	0	
H9281B		2 X 8 backplane			2.4	0	
H9281C		2 X 12 backplane			3.6	0	
IBV11-A	M7954	Instrument bus interface	0.8 A	–	1.9	1	Double
KD11-F	M7264	LSI-11 CPU with 4K RAM	1.8 A	0.8 A	2.4	1	Quad
KD11-H	M7264-YA	LSI-11 CPU without RAM	1.6 A	0.25 A	2.4	1	Quad
KD11-HA	M7270	LSI-11/2 CPU	1.0 A	0.22 A	1.7	1	Double
KDF-11	M8186	LSI-11/23 CPU	2.0 A	0.2 A	2.0	1	Double
KDF-11B	M8189	PDP-11/23-PLUS CPU with bootstrap, LTC, and two SLUs	4.5 A	3 A	2.0	1.0	Quad
KUV-11	M8018	WCS module	3.0 A			1	Quad
KPV11-A	M8016	Power-fail/line-time clock	0.56 A	–	1.63	1	Double
KPV11-B	M8016-YB	Power-fail/line-time clock/120 Ω bus terminator	56 A	–	1.63	1	Double
KPV11-C	M8016-YC	Power-fail/line-time clock/220 Ω bus terminator	0.56 A	–	1.63	1	Double
KWV11-A	M7952	Programmable real-time clock	1.75 A	0.01 A	3.4	1	Quad
KWV11-C	A4002	Programmable real-time clock	1.75 A	0.1 A	1.0	1.0	Double
KXT11-AA	M8063-AA	Single board computer	2.8 A	1.10 A	1.7	1	Double
LAV11	M7949	LA180 line printer interface	0.8 A	–	1.8	1	Double
LPV11	M8027	LA180/LP05 printer interface	0.8 A	–	1.4	1	Double
MCV11-D	M8631	8K X 32KB CMOS read/write memory	1.20 A		2.0	1.0	Dual
MRV11-AA	M7942	4K X 16 read-only memory (less PROM integrated circuits)	0.4 AA	–	1.8	1	Double
		(with 32 512 X 4 PROM integrated circuits) (MRV11-AC)	2.8 A				
MRV11-BA	M8021	UV PROM-RAM (less PROM integrated circuits)	0.58 A	0.34 A			
		(with 8 1K X 8 PROM integrated circuits) (MRV11-BC)	0.62 A	0.5 A			
MRV11-C	M8048	PROM/ROM module	0.8 A				
MSV11-B	M7944	4K X 16 read/write MOS memory	0.6 A	0.54 A			
MSV11-CD	M7955-YD	16K X 16 read/write MOS memory	1.1 A	0.54 A			
MSV11-D	M8044	4K/16K/32K MOS memory	1.7 A	0.34 A			
MSV11-E	M8045	4K/16K/32K MOS memory	2.0 A	0.41 A			
MSV11-L	M8059	256K memory	4.02 A	–			
MSV11-P	M8067	128K/256K X 16 read/write MOS memory	3.45 A				
MXV11-A	M8047	Multifunction module	1.2 A	0.1 A			
REV11-A	M9400-YA	120 Ω terminator, DMA refresh, bootstrap ROM	1.6 A	–			
REV11-C	M9400-YC	DMA refresh, bootstrap	1.6 A	–			
RKV11-D	M7269	LSI-11 Bus control for RKV11-D	1.8 A	–			
RLV11	M8013 M8014	RL01 disk drive	6.5 A	1.0 A			
RLV12	M8061	Disk controller	5.0 A	0.1 A			
RXV11	M7946	RX01 interface	1.5 A	–			
RXV21	N8029	Double density floppy interface	1.1 A				
TEV11	M9400-YB	120 Ω terminator	0.5 A	–			
TU58		Serial/cartridge cassette	0.75 A Appr	1.2 A max			
VK170	CAM7142	Serial video module	1.2 A	0.15			

PDP-11

SYSTEM SOFTWARE

RT-11	Real-Time Operating System for PDP-11 Processors. A small, single-user foreground/background system that can support a real-time application job's execution in the foreground and an interactive or batch program development job in the background.
DSM-11	DIGITAL Standard Mumps Operating System for PDP-11 Processors. A small to large sized timesharing system that offers a unique fast access data storage and retrieval system for large data base processing.
RSTS/E	Resource-sharing Timesharing System/Extended Operating System for PDP-11 Processors. A moderate to large sized timesharing system that can support up to 63 concurrent jobs, which includes interactive terminal user jobs, detached jobs, and batch processing.
RSX-11M	Real-Time Multiprogramming Executive Operating System for PDP-11 Processors. A small to moderate sized real-time multiprogramming system compatible with RSX-11D that can be generated for a wide range of application environments — from small, dedicated systems to large, multi-purpose real-time application and program development systems.
RSX-11S	Real-Time Multiprogramming Executive Operating System for PDP-11 Processors. A small, execute-only member of the RSX-11 family for dedicated real-time multiprogramming applications (requires a host RSX-11M or VMS system).
IAS	Interactive Application System for PDP-11 Processors. A large, multi-user timesharing system, allowing real-time applications execution concurrent with timeshared interactive and batch processing.

LANGUAGE TABLE

MACRO	RT-11, RSX-11, RSX-11D, IAS, TRAX, VAX/VMS
FORTRAN 1V	RT-11, RSX-11, RSX-11D, IAS, RSTS/E VAX/VMS
FORTRAN 1V-PLUS	RSX-11, RSX-11D, VAX/VMS
BASIC-11	RT-11, RSX-11, IAS
BASIC PLUS-2	RSX-11, RSX-11D, IAS, TRAX, VAX/VMS
BASIC-PLUS	RSTS/E
RPG11	RSX-11M, RSTS/E
DIBOL	RT-11 RSTS/E
COBOL	RSX-11, RSX-11D, RSTS/E, TRAX, VAX/VMS

LSI-11 BASED 11/04 11/34 11/45 11/55 11/60 11/70	**RT-11 Foreground/Background or Single-Job Operating System** 16K to 256K bytes of memory. In 16K bytes: Single-Job (SJ) operation; subset MACRO included; BASIC, FORTRAN IV, FOCAL as options. In 32K bytes: Foreground/Background (FB) or SJ operation; languages can support string operations, laboratory and graphics peripherals; full MACRO assembler included; multi-user BASIC available as option supporting as many as 4 users (under SJ monitor). MU BASIC supports as many as 8 users in 48K bytes under SJ monitor and as many as 4 in 56K bytes under FB monitor. Languages: MACRO included; FORTRAN IV; BASIC, MU BASIC, FOCAL, and APL are options
11/04 11/34 11/45 11/55 11/60 11/70	**DSM-11 DIGITAL Standard MUMPS-11 (Multi-User)** 64K to 1Mb of memory. 64K bytes will allow approximately 2 to 4 users to operate simultaneously. A maximum of 63 jobs may be supported depending on processor and partition size, supports many users accessing a common data base for easy applications development. Languages: DSM-11 included.
11/34 11/45 11/55 11/60 11/70	**RSTS/E General Purpose Timesharing System** 96K to 248K bytes of memory, or 96K to 3840K bytes on 11/70. Depending on disk and memory configuration, RSTS/E can support a maximum of 63 jobs. Languages: BASIC-PLUS and MACRO included; COBOL, BASIC-PLUS-2, FORTRAN IV, DIBOL, RPG II, DATATRIEVE-11, and APL are options.
LSI-11 BASED 11/04 11/34 11/45 11/55 11/60 11/70 VAX-11/780	**RSX-11S Execute-Only Real-Time Multi-Programming System** 16K to 3840K bytes of memory. 8K-byte system allows 4K for user tasks. 16K bytes required for on-line task loading or support for tasks written in FORTRAN. Languages: Program development on host RSX-11D/M, IAS, or VAX/VMS.

11/04
11/34
11/55
11/60
11/70

RSX-11M Small-to-Moderate-Sized Real-Time Multi-Programming System

32K to 248K bytes of memory or 32K to 3840K bytes on 11/70. At least 48K bytes are required for full MACRO support, concurrent program development and application tasks execution or memory management support. Error logging supported.

Languages: MACRO included; FORTRAN IV and FORTRAN IV-PLUS, BASIC, BASIC-PLUS-2, COBOL, RPG, DATATRIEVE, and CORAL 66 are options.

11/45
11/55
11/60
11/70

IAS Multi-Purpose Multi-Programming System

128K to 248K bytes of memory or 128K to 3840K bytes on 11/70. Timeshared interactive and batch job processing with concurrent real-time applications execution. Depending on disk and memory configuration, as many as 10 interactive users can be supported on an 11/60; as many as 20 interactive users on an 11/70. Error logging supported.

Languages: MACRO included; FORTRAN IV, FORTRAN IV-PLUS, COBOL, BASIC, BASIC-PLUS-2, RPG, and CORAL 66 are options.

11/04
11/34
11/45
11/60
11/70

TRAX Dedicated Transaction Processing System

192K to 3840K bytes on 11/70. Interactive transaction processing characterized by sets of predefined procedures with multi-user protection built in.

Languages: COBOL, BASIC-PLUS-2, FORTRAN IV, APL, and DATATRIEVE are options.

OPERATING SYSTEMS

RT-11	RSTS/E	RSX-11M
Is • Foreground/ background (multi-tasking) • Single user • Sensor based • Operating on small CPUs • Protected environment • Easy to install and use • High real-time throughput • Batch processing • Highly reliable • Full development facilities	**Is** • General purpose timesharing • High performance timesharing BASIC • Interactive environment • Multi-language • Batch processing • Basis of most commercial applications	**Is** • Real-time processing • Sensor based • Data base management • Multi-user development • Building block operating system for: - Communications - Commercial applications - Turn-key applications
Is not • Transaction processing • Record management • Data base management	**Is not** • Real-time • High volume transaction processing • Block mode application terminals	**Is not** • Batch processing • Timesharing • Protected environment
	Includes Data Mgr./ Utilities • RMS-11 • SORT-11 • DATATRIEVE-11 • DMS-500	**Includes Data Mgr./ Utilities** • RMS-11 • DBMS • DATATRIEVE-11 • SORT-11
Languages • BASIC-11 • FORTRAN IV • MACRO-11 • FOCAL • APL	**Languages** • BASIC-PLUS • BASIC-PLUS-2 • COBOL • FORTRAN IV • MACRO-11 • RPG II • DIBOL-11	**Languages** • COBOL • FORTRAN IV • FORTRAN IV-PLUS • MACRO-11 • BASIC-11 • BASIC-PLUS-2 • RPG II

OPERATING SYSTEMS

IAS	DSM-11	TRAX-11
Is • Real-time • Timesharing • Batch processing • Data base management • Multi-function • Multi-language • Extensible executive • High RSX/VAX/ TRAX compatibility • Protected environment	**Is** • Interactive, high-productivity applications development for data base management system • Highly approachable • Integrated language/command environment • Powerful language structure for text processing • Large numer of terminals—up to 80	**Is** • High volume transaction processing • Batch processing • Protected environment • Application development tools: - Debug utility - Terminal screen language • Distributed functionality • RSX/VAX compatibility • Easy systems design
Is not • High capacity (dedicated) timesharing • High capacity (dedicated) real-time • Operating on small CPUs	**Is not** • General timesharing • Real-time • Computational or batch • Multi-language	**Is not** • Timesharing • Sensor based • For smaller CPUs • Large scale batch (IBM)
Includes Data Mgr./ Utilities • DBMS • RMS-11 • DATATRIEVE-11 • SORT-11		**Includes Data Mgr./ Utilities** • RMS-11 • DATATRIEVE-11 • SORT-11
Languages • BASIC-11 • BASIC-PLUS-2 • COBOL • FORTRAN IV • MACRO-11	**Languages** • DSM-11	**Languages** • COBOL • BASIC-PLUS-2 • MACRO-11

SECTION 10

D.E.C. V.D.U's

VT50 - 12 Line x 80 character 5 x 7 Dot Matrix
Blinking underline cursor
Power on - R.H. side
Contrast adjust - sliding Pot L.H. rear
Baud Rate Set via two rotary switches accessible through bottom plate
Basic = Current Loop : E.I.A. optional
Terminal is a passive Device
Normally used with no parity
ESCH.ESC J clears the screen

VT52 - 24 line version of VT50

VT55 - VT52 with Graphics Option

VT100 - MicroProcessor controlled VDU - All parameters are set by software : Consult terminals handbook
Run's on internal self test on Power on
EIA : Standard

VT132 - VT100 with AVO option, printer port and Edit firmware

VT105 - VT100 with M7071 wareform generator

VT125 - VT100 with intelligent graphics processor

VT640 - VT100 with tektronix compatible retrographic processor

VT101 - The VT101 is a new generation VDU based on the VT100 design principles - Bounded Terminal no options can be installed
VT101 = Basic VT100

VT102 - Bounded Terminal with AVO printer port Half Duplex modem control as standard

VT131 - As VT102 plus Edit Firmware

NB The 101 family is based on the same logic PCB, firmware changes between model numbers

There is NO hardware compatibility between the VT100 and VT101 families

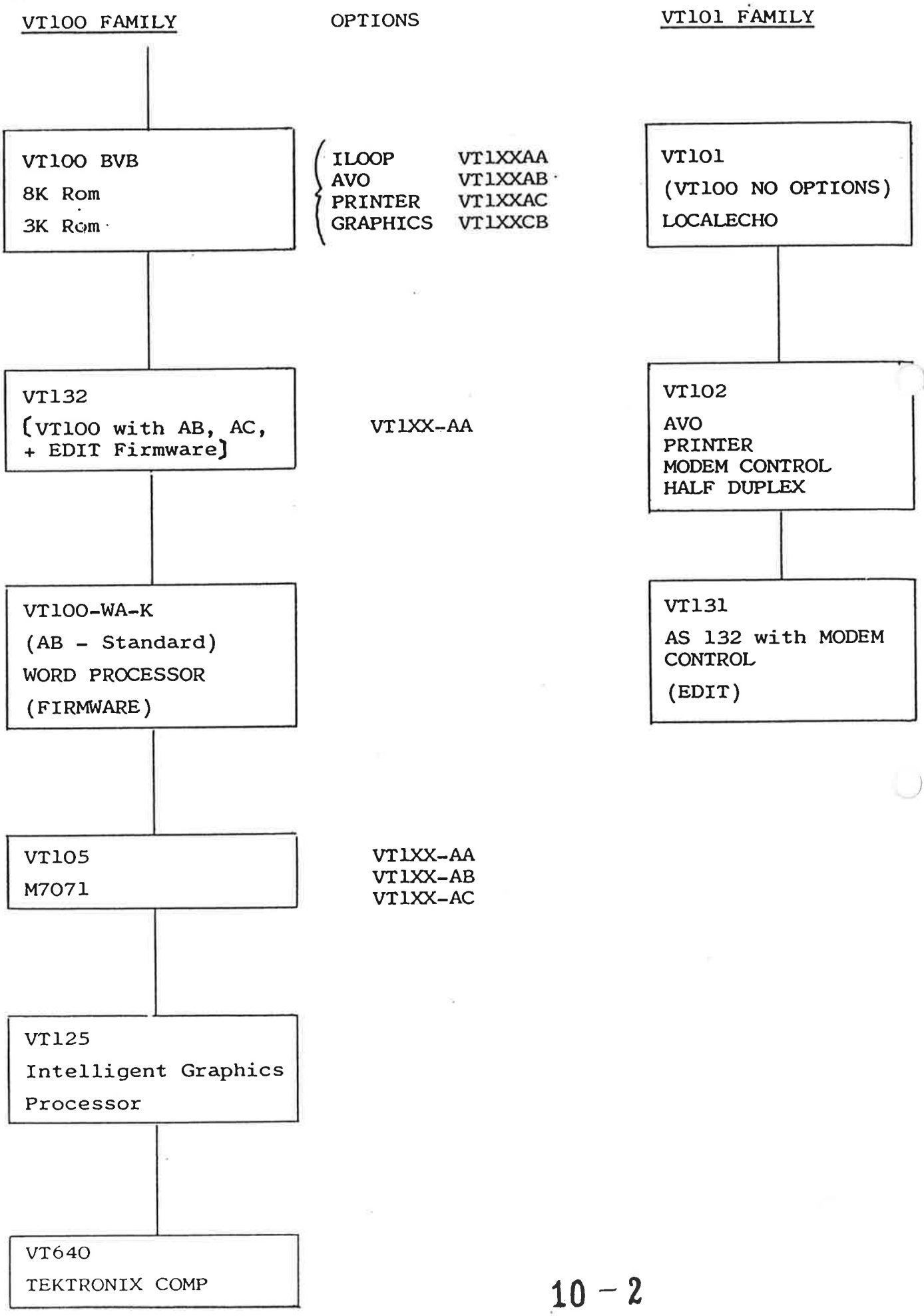
INTELLIGENT TERMINALS

VT103 - Basic VT100 plus LSI-11 backplane. TU58/RX02

PDT11/-110 - VT100 - LSI-11 processor, up to 60KB memory, Asynchronous communications port

PDT11/-130 - As above with TU58

PDT11/-150 - RX01 and LSI system interfaced to VT100


VT100 FAMILY
OPTIONS
VT101 FAMILY
VT100 BVB
8K Rom
3K Rom
ILOOP VT1XXAA
AVO VT1XXAB
PRINTER VT1XXAC
GRAPHICS VT1XXCB
VT101
(VT100 NO OPTIONS)
LOCALECHO
VT132
(VT100 with AB, AC,
+ EDIT Firmware)
VT1XX-AA
VT102
AVO
PRINTER
MODEM CONTROL
HALF DUPLEX
VT100-WA-K
(AB - Standard)
WORD PROCESSOR
(FIRMWARE)
VT131
AS 132 with MODEM
CONTROL
(EDIT)
VT105
M7071
VT1XX-AA
VT1XX-AB
VT1XX-AC
VT125
Intelligent Graphics
Processor
VT640
TEKTRONIX COMP

PRINTING TERMINALS

	DECWRITER I	DECWRITER II	DECWRITER III	DECWRITER III	DECWRITER IV	DECPRINTER I
	LA30	3 LA35/36	LA120	LS120	4 LA34/38	LA180
PRINT SPEED	30CPS	30CPS	180CPS	180CPS	30CPS	180CPS
COLUMNS	80	132	1 132	1 132	1 132	132
CHARACTER MATRIX	7 x 7	7 x 7	7 x 7	7 x 7	7 x 9	7 x 7
BAUD RATES	110 300	110 150 300	110 - 9600	110 - 9600	110 300	2 110 - 9600
E.I.A.	OPTION	OPTION	STANDARD	STANDARD	STANDARD	OPTION
CURRENT LOOP	STANDARD	STANDARD	OPTION	OPTION	NONE	OPTION PARALLEL STANDARD
MODEM CONTROL	BASIC	OPTION	STANDARD	STANDARD	BASIC	STANDARD
SET UP FEATURE	NO	NO	YES	YES	YES	NO
LOGIC P.C.B's	-	M7728	M7081	PRINTER LOGIC 54-11023 LS120 - 54 - 12610	54-13374	PRINTER LOGIC 54-11023
COMMENTS		3 LA35 IS R.O.		1 CHARACTER SPACING IS PROGRAMMABLE	TRACTOR STANDARD	2 SERIAL I/O

LINE PRINTERS

	LP11-A	LP11-B	LP11-EA	LP11-EB	LP11-C	LP11-D	LP11-Y	LP11-Z	LXY11	LXY21
TYPE	DATA BAND B300	PRODUCTS BAND B300	DATA BAND B600	PRODUCTS BAND B600	DRUM	DRUM	DRUM	DRUM	PRINTRONICS DOT MATRIX P300	PRINTRONICS DOT MATRIX P600
PRINTING SPEED 96-CHAR. SET 64-CHAR. SET	N/A 300 l/min	215 l/min 300 l/min	N/A 600 l/min	445 l/min 600 l/min	N/A 900 l/min	660 l/min N/A	N/A 600 l/min	436 l/min N/A	300 l/min N/A	600 l/min N/A
PVFU	NONE	NONE	NONE	NONE	NONE	NONE	OPTIONAL	OPTIONAL	STANDARD	STANDARD
OPTIONAL CHARACTER SETS	YES	YES	YES	YES	NO	NO	NO	NO	YES	YES
PLOT CAPABILITY	NO	NO	NO	NO	NO	NO	NO	NO	YES	YES
UNIBUS INTERFACE	M7930 M7258	-LA11 -LP11	M7258	M7258	M7258	M7258	M7258	M7258	M7258	M7258
Q-BUS INTERFACE	M7949 M8027	-LAV11 -LPV11	M8027	M8027					M8027	M8027

RUNNING INSTRUCTIONS FOR B600 BAND PRINTER

1. Switch Power on.
2. Ensure green Power light illuminated.
3. Ensure red alarm light goes out after 10 seconds.
4. Set up top of form.
5. Select on line. Ensure green on line light illuminates.

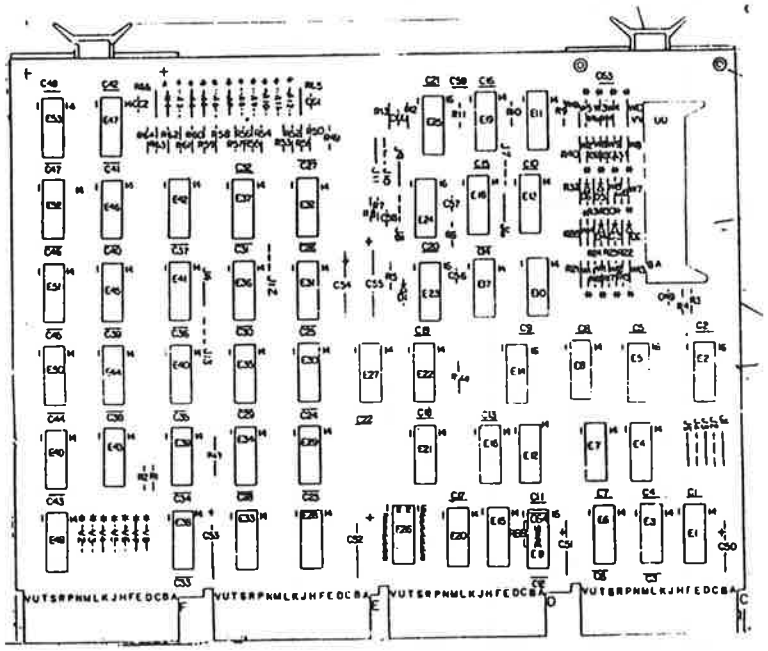
Line Printer Interface - M7258

Base ADD: 777514 CSR -

516 BUFF -

VECTOR: 200

QUAD Height PCB any SPC SLOT.



JUMPER TABLE				
JUMPER DESIGNATION	UNIT NO. LSII	LVII	LPII	LAII
J1	OUT	IN	OUT	IN
J2	IN	OUT	IN	OUT
J3	IN	IN	IN	IN
J4	OUT	OUT	OUT	OUT
J5	IN	IN	IN	IN
J6	IN	OUT	IN	IN
J7	OUT	IN	OUT	OUT
J8	OUT	IN	IN	OUT
J9	IN	OUT	OUT	IN
J10	OUT	IN	OUT	OUT
J11	IN	OUT	IN	IN
J12	OUT	OUT	OUT	OUT
J13	OUT	OUT	OUT	OUT
W9	IN	IN	IN	IN
W5	OUT	IN	OUT	OUT
W4-W9, W6-W15	IN	IN	IN	IN
N1	IN	IN	IN	IN

CARD READERS

	CR11(-A)	CR11-B	CMS11-K/CME11-K
CARD TYPE	HOLE PUNCHED	HOLE PUNCHED	HOLE PUNCHED OR MARK SENSE
CARD RATE	285	600	250
INPUT HOPPER/ OUTPUT STACKER CAPACITY	550	1000	200

PC11

Paper Tape Reader/Punch

Module	Description	Bin	Location
M781	PC11 Control Board	20309	C-D 3-9
M105	Address Decoder	4568	E 3-9
M7820	Interrupt Controller	20310	F 3-9

New version PC11 Controller - Single Quad height board:-

M7810	PC11 Interface	32781	C-F 3-9

Base Address: 777550 M105 In=Ø

Base Vector 70 M7820 In=1

XXDP DIAGNOSTIC IDENTIFICATION

1 XXDP (OLD STYLE)

i) XXDP.SAV monitors (i.e. RKDP.SAV)

ii) Help message is printed out when monitor is loaded from medium.

iii) Date is requested when using UPD1/UPD2.

2 XXDP+ V1.0

i) HMXXrp.SYS monitors (i.e. HMDKA0.SYS)

ii) Loaded monitor asks for date, Hertz and type of bus on system.

iii) UPD1/UPD2 will not ask for date.

iv) The following output is printed by the loaded monitor:

```
CHMDKA0 XXDP+ DK MONITOR nnk
BOOTED VIA UNIT :  0

RESTART ADDRESS :  nnnnnn

50 HZ ?   N
LSI ?     N
```

where - nnk is the memory size (up to 28K)

- CHMDKA0 is the loaded monitor.

3 XXDP+ V1.1 (called plus-plus or super-plus)

i) Loaded monitor will ask for date but not Hertz

ii) Loaded monitor will ask for type of bus only if 11/23 - 11/24 system.

iii) Monitor command "TEST" will run a batch file "SYSTEM.CCC"

iv) The following output is printed by the loaded monitor:

```
CHMDKB0 XXDP+ DK MONITOR
BOOTED VIA UNIT 0
nnk UNIBUS SYSTEM

DATE (dd-mmm-yy)

RESTART ADDRESS:  nnnnnn
```

where - nnk is the memory size (up to 28K)

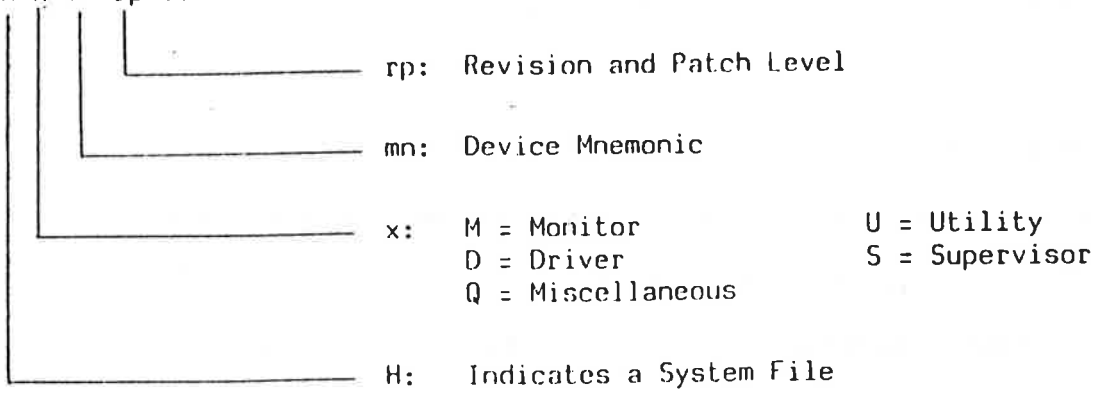
- CHMDKB0 is the loaded monitor.

XXDP - FILE IDENTIFICATION

NAMING

.SYS FILES

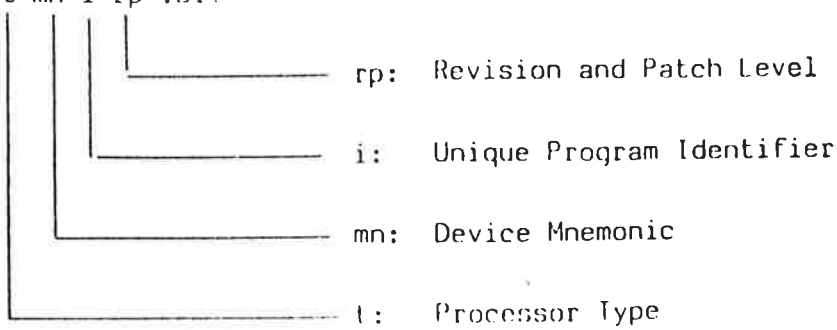
H x mn rp .SYS i.e: HMDMA0.SYS



Directory Utility File	HUDIrp.SYS
Setup Utility File	HUSUrp.SYS
XXDP Supervisor File	HSAArp.SYS
PT/AMS Supervisor File	HSABrp.SYS
User Manual	HQSArp.SYS

.BIN, .BIC, .OBJ FILES

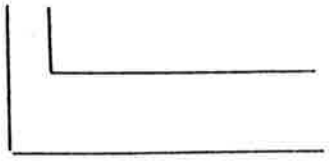
t mn i rp .BI? i.e: ZDHAC0.BIC



NAMING (Continued)

XXDP

XX DP.??? i.e: RKDP.SAV

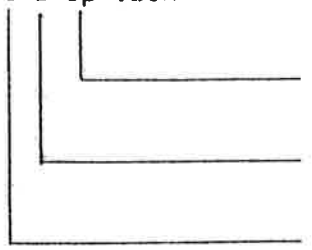


This naming convention is used on three types of files:

- Old style monitor/bootstrap program i.e. RKDP.SAV
- Old style directory text file i.e. RKDP.DIR
- Distribution media i.e.: RKDP - XXDP on RK05 disk cartridge

INSTRUCTION/UNIBUS

D t i rp .BIN i.e: D0AA0.BIN



0 = Instructions Test
1 = Addressing Test
6 = AA11/VT06/LAB-11 Test
8 = Unibus Test

OTHERS

COPY .BIN	XXDP Copy Program
DXCL .BIN	DEC/X11 Configurator and Linker
HELP .TXT	Help Text File
PATCH .BIN	XXDP Patch Program
SETUP .BIN	Diagnostic Routine Services Setup Program
UPDn .BIN	XXDP Update Program, n = 1, 2, 3
XTECO .BIN	XXDP Text Editor
XXBLD .BIN	Build Utility Chain File
nDIREC .TRY	Directory Text File n = 1, 2, 3 ...

Non DEC programs and files will employ the same naming conventions, but there may be some that use Obvious English words or synonyms, i.e. FLOPPY.BIN or TYPE.ME

PROCESSOR TYPES

A = 11/05, 15, 20
B = 11/40
C = 11/45
D = GT40, Instruction/Unibus Tests
E = 11/70
F = 11/34
G = 11/04
H = System files
J = 11/23, 24
K = 11/44
M = MNC-11
N = System Industries 9400 Controller Diagnostics
P = PDT-11, Plessey Diagnostics
Q = 11/60
R = LPA-11
T = .MPG Files
V = 11/03
X = DEC/X11 Object Files
Z = Any Processor

EXTENSIONS

.BIC	Binary image file (Chainable)
.BIN	Binary image file
.CCC	Batch Chain file
.DIR	Directory text file; File created by DIR command
.MPG	
.OBJ	DEC/X11 OBJect file
.SAV	Memory image file; File created by SAVE/SAVM command
.SYS	System file
.TRY	Directory text file
.TXT	Text file

DIAGNOSTIC RUNTIME SERVICES - DRS

PROMPT

DR> - Issued when program started, ^C detected or 'halt-on-error' condition.

EXECUTION

STA	START	-	Start the diagnostic and initialize.
RES	RESTART	-	Start diagnostic and do not initialize.
CON	CONTINUE	-	Continue diagnostic from ^C
PRO	PROCEED	-	Continue from an error halt

UNITS UNDER TEST

DRO	DROP	-	Deactivate a unit.
ADD	ADD	-	Activate a unit for testing.
DIS	DISPLAY	-	Print a list of device information.

FLAGS

FLA	FLAGS	-	Print status of all flags.
ZFL	ZFLAGS	-	Reset (clear) all flags.

STATISTICS

PRI	PRINT	-	Print statistical information.

EXIT

EXI	EXIT	-	Return to XXDP+ runtime monitors

SWITCHES

Note: ddddd = 1 to 65536

/TESTS : testlist	-	Execute only tests specified.
/PASS : ddddd	-	Execute ddddd passes
/FLAGS : flaglist	-	Set specified flags.
/EOP : ddddd	-	Report end of pass after each ddddd passes.
/UNITS : unitlist	-	Command will only affect specified units.

	/TESTS	/PASS	/FLAGS	/EOP	/UNITS
START	x	x	x	x	x
RESTART	x	x	x	x	x
CONTINUE		x	x	x	

SWITCHES (Continued)

	/TESTS	/PASS	/FLAGS	/EOP	/UNITS
PROCEED			x		
DROP					x
ADD					x
PRINT					
DISPLAY					x
FLAGS					
2 FLAGS					
EXIT					

Examples: STA/UNIT:1-4/TES:1:5:15/PASS:100/EOP:10
CON/FLAGS:LOE:IER
RES/TESTS:1:3-6:8

FLAGS

HOE - Halt on Error
LOE - Loop on Error
IER - Inhibit all error reports
IBE - Inhibit all error reports except first level (Basic report)
IXE - Inhibit extended error reports
PRI - Direct messages to line printer
PNT - Print test number as test executes
BOE - "Bell" on error
UAM - Unattended mode (no manual intervention)
ISR - Inhibit statistical reports
IDU - Inhibit program dropping of units
ADR - Execute autodrop code
LOT - Loop on test
EVL - Execute evaluation

SETUP

SETUP.BIN is a utility file that will build the hardware and software tables for a diagnostic, prior to running that diagnostic.

Setup will ask for the target environment for the diagnostic - XXDP or ACT-11.

SETUP COMMANDS

SETUP - Build tables for specified diagnostic.
SETUP [DEVo:] OUTFILE = [DEVI:] INFILE
If INFILE = OUTFILE will ask to delete INFILE

LIST - Lists all DRS diagnostics on medium
LIST [DEV:] [FILENAME]

EXIT - Return control to XXDP+

BUILDING A CHAIN FILE

1)	Boot Device	DM
2)	Run the TEXT EDIT program utility	R XTECO
3)	Create a new TEXT file on SELECTED DRIVE	TEXT DMØ: FILNAM.CCC
4)	The program will then respond with a Prompt	"
5)	INSERT TEXT USING XTECO Command Format (I = INSERT TEXT etc)	
6)	Terminate command string	ESC ESC
7)	Exit XTECO and write file to disc	EX ⟨ESC⟩⟨ESC⟩

EDITING AN EXISTING FILE

1)	Run the TEXT EDIT UTILITY	R XTECO
2)	Obtain file from Disc	TECO DMØ:FILNAN.CCC
3)	Use XTECO commdands to DELETE and INSERT TEXT	
4)	Terminate command string	⟨ESC⟩⟨ESC⟩
5)	Exit XTECO and write updated file to Disc	EX ⟨ESC⟩⟨ESC⟩

BUILDING A DECX11 R.T.E.

1)	List all the devices on the system requiring test	
2)	Select required modules from object files	
3)	Map address vectors and SR's from cross reference manual	
4)	Run DECX11 configurator/Linker	R DXCL
5)	Enter configure mode	CNF
6)	Enter monitor required on promt	C
7)	Enter modules required	MDL KWAGØ
8)	EXIT configure mode	EX
9)	SAVE configuration table	SAVC DKØ:X11CN1.CNF
10)	Link configuration table and monitor	LINK DKØ:X11CN1.BIN= DKZ: XMONCØ.LIB
11)	Return to monitor	EXIT
12)	Run R.T.E.	R X11CNI
13)	Command mode	RUN

DECX11

ADDING NEW MODULES

1)	RUN DECX CONFIGURATOR/LINKER	R DXCL
2)	GET THE CONFIGURATION TABLE FROM DISC	GETC X11CN1 CNF
3)	DISPLAY CONFIGURATION TABLE	PRINT C
4)	ENTER CONFIGURATION MODE	CNF
5)	ADD NEW MODULE	MDL TMAJ
6)	EXIT CONFIGURATION MODE	EX
7)	SAVE NEW CONFIGURATION TABLE	SAVC DKO: X11CNZ•CNF
8)	LINK NEW EXERCISER	LINK DKO: X11342•BIN= DKO: XMONCO•LIB
9)	EXIT DECX	EXIT
10)	RUN EXERCISER	R X11342

SYSTIME

Systime is a DEC based O.E.M. company producing a variety of RSTS/E based systems.

The processing hardware of these systems is a hybrid of DEC processor PCB's and backpane plus systime manufactured memory S.L.U's and Disc Controllers.

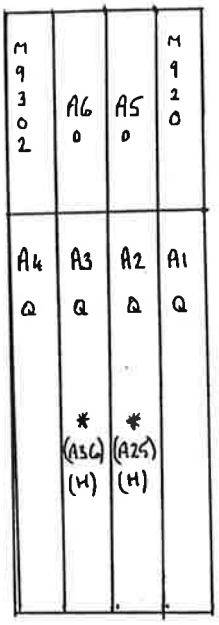
Systimes design and operating Spec's are in the main compatible with DEC's original design and register assignments.

Systime produce the following systems for U.K. Sale.

System	DEC CPU	Disc Subsystem
1000	1104	5301/RK/AMPEX
3000*	1104	5301/RP
5000	1134	5310/5311/SMD
6000	1160	
6700	1170	
6400	1144	

*There is a modified 3000 system available with extended memory control (EMC) comprising controller 9 slot backplane and memory. This modification allows addressing capability of up to 128KW.

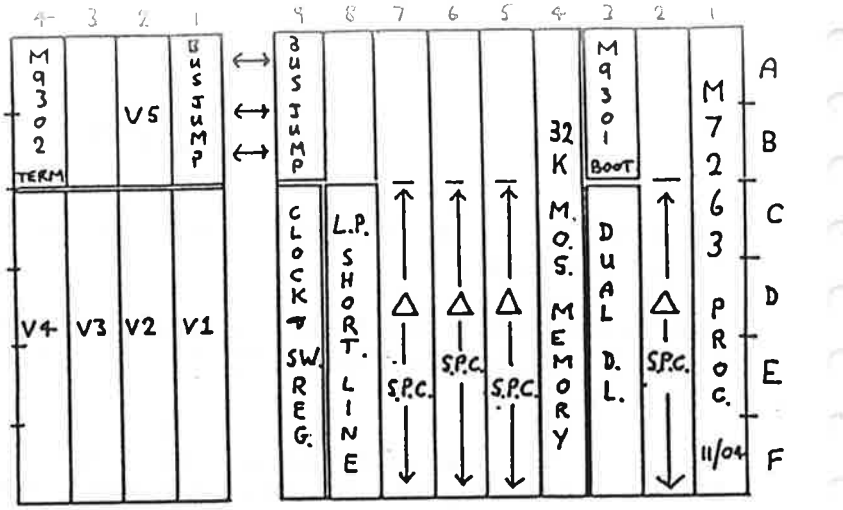
SYSTIME 5311



BACKPLANE part no 50-0119
Bin 31969

Supports CDC 9760/40MB
9762/80MB

* 2 versions 4 PCB / 6 PCB



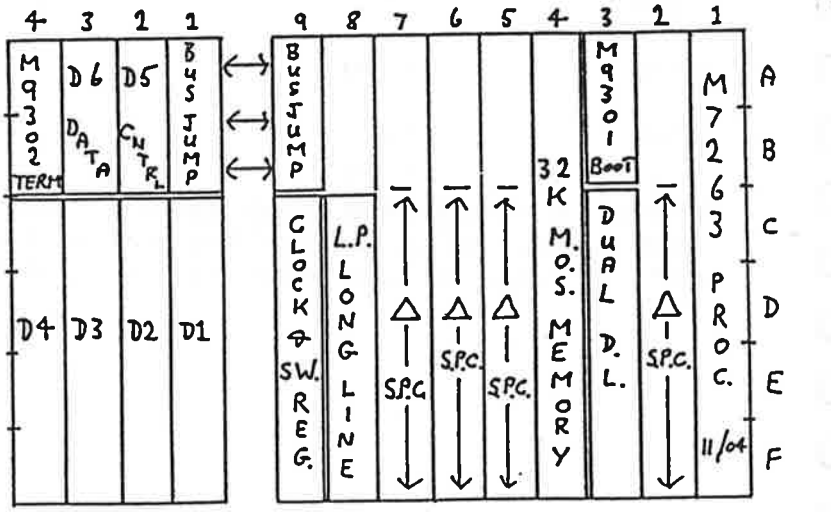
5301 (RK)

M.U.D. BACKPLANE

△ = B.G. CARD IF NO S.P.C. FITTED

(V5 ONLY USED IF DRICO DRIVES ARE USED)

SERIES 3000 MAP

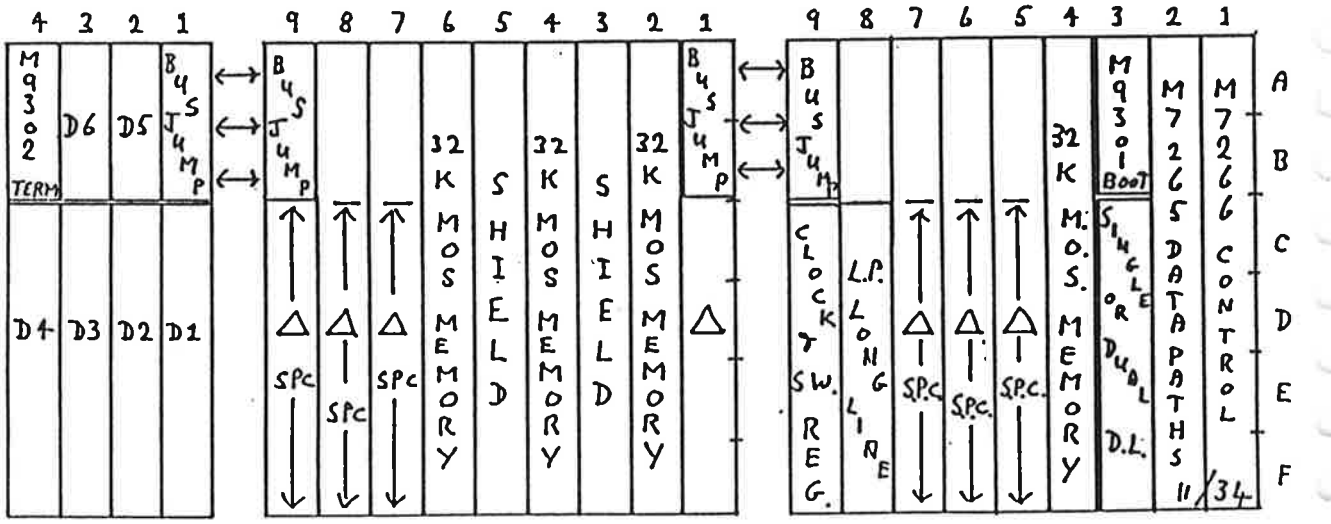


5310 (RP)

M.U.D BACKPLANE

NOTE :- MAY HAVE EXTRA S.P.C.'s IN SLOTS 5, 6, 7

SERIES 5000



5310

S.P.C. BACKPLANE

M.U.D. BACKPLANE

5310 WILL PROBABLY HAVE 2 CDC 9746 40M/B DRIVES

SERIES 3000 - EXTENDED VERSION

In order to extend the 32K word addressing capability of the 11/04, the Systime extended memory interface board can be fitted thus giving the system full addressing capability up to 128K words.

In the modified 3000 configuration there is no memory installed in the processor backplane. Instead, a special 9 slot backplane is installed on the uni-bus after the disc control. The special backplane is mapped as follows:-

Slot 1	=	Extended memory unit
Slot 2	=	32K MOS Memory
Slot 3	=	Memory shield
Slot 4	=	32K MOS Memory
Slot 5	=	Memory shield
Slot 6	=	32K MOS Memory
Slot 7	=	Memory shield
Slot 8	=	32K MOS Memory
Slot 9	=	M9302 Bus terminator

Series 5000 LARGE VERSION.

There are some larger configurations in the field which have two S.P.C. 9 slot backplanes followed by a bus repeater and more S.P.C. backplanes.

DISC SYSTEMS SUMMARY

5301 (RK)

Handle code:-

V1 = White top row, violet all others.

V2 = White 2nd row, " " "

V3 = White 3rd row, " " "

V4 = White 4th row, " " "

V5 = 2 violets (2.4m/b version)

or V5 = White/Violet (4.8m/b version)

5301 control supports:- 2.4m/b Drico Series 30, or RK05
4.8m/b Drico Series 3200.

5310 (RP)

Handle code:-

D1 = White top row, blue all others.

D2 = White 2nd row, " " "

D3 = White 3rd row, " " "

D4 = White 4th row, " " "

D5 = Co-Ax and twisted pairs.

D6 = Twited pairs only.

5310 control supports:- Memorex 660 - 20 m/b
C.D.C. 9746 - 40 m/b.

5311 (S.M.D).

Handle code:- A1 = White top row, red all others
A2 = White 2nd row, " " "
A3 = White 3rd row, " " "
A4 = White 4th row, " " "
A5 Has the TO3 driver can
A6 Has just chips.

Supports:- C.D.C. 9760 20m/b. 132
C.D.C. 9762 40m/b. 164

SMALL PERIPHERAL CONTROLS.

Single DL11, Handle code:- all brown, supports 1 EIA/20 mA Loop device

Dual DL11, Handle code:- all black, supports 2 E.I.A. devices

Quad DL11, Handle code:- all black, supports 4 E.I.A. devices

L.P. SHORT LINE, Handle code:- Red 2nd row, all others orange
Supports:- Drico 6330 or 6320,
C.D.C. 600 L.P.M. (with jumper changes).

MEMORY 32K MOS, handle code all green.
Memory shield, handle code, row 1 white, green all others.

MEMORY EXTENDER Row 1 = white, green all others.

SWITCH REG AND CLOCK.

Handle code:- BERG, green, yellow, green.

Provides external switch register interface via Berg connector. A mains frequency clock is also included which is compatable with D.E.C. KW11 - L.

MEMORY TYPES

SYSTIME 32K M.O.S.

This board has one switch of two contacts to select stack starting address. Contact positions are as follows:-

S1	S2	Starting Addr.
off	off	0 - 32K
on	off	32 - 64K
off	on	64 - 96K
on	on	96 - I28K

DEC MS II

If DEC I6K M.O.S. or core memory boards are encountered the instructions for configuring switches and jumpers will be found in the II/04, /34 Maintenance card supplied with this book.

DIAGNOSTICS

R.P.

ZRPBTF	RP 11 C Reliability (20 & 40 MB)
ZRPSMD	S.M.D. Reliability (16, 32 & 64 MB)
ZRPCIS	RP 11 Multi-Disc (20 & 40 MB)
ZRPSMM	S.M.D. Multi-Disc (16, 32 & 64 MB)

R.K.

ZRKHF0	RK 11/RK 05 Performance Exerciser
ZRKIAS	RK 11/RK 05 Utility Package
ZRKJD0	RK 11/RK 05 Basic Logic Test 1
ZRKKD0	RK 11/RK 05 Basic Logic Test 2
ZRKLD0	RK 11/RK 05 Dynamic Test

SYSTIME MODEL CROSS REFERENCE

MODEL	DESCRIPTION
5264	32KW MOS MEMORY
5265	64KW MOS MEMORY
5300	DISC CONTROLLER FOR 5304 (AMPEX 10MB)
5301	DISC CONTROLLER FOR 5305 (DRICO 2.4MB)
5304	DISC DRIVE AMPEX 443
5305	DISC DRIVE DRICO 2.4MB
5310	DISC CONTROLLER FOR MEMOREX 660/CDC 9746 (RP02/03)
5311	DISC CONTROLLER FOR 5361/5360
5360	DISC DRIVE CDC 9760 16MB
5361	DISC DRIVE CDC 9760 32MB
5362	DISC DRIVE CDC 9762 64MB
5363	DISC DRIVE CDC 9760 20MB
5364	DISC DRIVE CDC 9762 40MB
5736	DECWRITER - LA36
5760	VDU MK5 - SYSCOPE 500
5822	DUAL DL11
5827	QUAD DL11

SYSTIME PCB PART NUMBERS AND BIN'S

PART NUMBER	MODEL	DESCRIPTION	HANDLE CODE	BIN
30-1001		SINGLE LINE DL11-W		
30-0004	5820	SINGLE LINE DL11-E	BROWN	34381
30-0093	5822	DUAL LINE DL11	BLACK	35180
30-0120	5827	QUAD LINE DL11	BLACK	31024
	5828	Eight line DZ11		
30-0102		LP11-LONG LINE	ORANGE	34372
30-0107		LP11-SHORT LINE	ORANGE/RED 2nd	43353
30-5037	5264	32KW MOS MEM		29632
30-0201	5265	64KW MOS MEM		32050
30-0213	5265	64KW MOS MEM		
30-0114		32K MOS MEM		
30-0103	5301	V1	VIOLET/WHITE 1st	33827
30-0104	5301	V2	VIOLET/WHITE 2nd	
30-0104	5301	V2 (AMPEX 443)	VIOLET/BLACK 2nd	37449
30-0105	5301	V3	VIOLET/WHITE 3rd	33829
30-0106	5301	V4	VIOLET/WHITE 4th	33830
30-0193	5301	V5 (AMPEX 443)	VIOLET/BLACK	33832
30-0193	5301	V5 (DRICO2.4MB)	VIOLET/VIOLET	
30-0193	5301	V5 (DRICO4.8MB)	VIOLET/WHITE	
SUPPORTS:	RK05/DRICO SERIES	30/3200: AMPEX 443		
30-0097	5310	D1	BLUE/WHITE 1st	27155
30-0098	5310	D2	BLUE/WHITE 2nd	27156
30-0099	5310	D3	BLUE/WHITE 3rd	27157
30-0100	5310	D4	BLUE/WHITE 4th	27158
30-0088	5310	D5	COAX + TWISTED PAIRS (RADIAL)	27154
		D6	TWISTED PAIR ONLY (DAISY CHAIN)	
SUPPORTS:	MEMOREX 660/CDC 9746			
30-0157	5311	A1	RED/WHITE 1st	31968
30-0192	5311	A2	RED/WHITE 2nd	32422
30-0185	5311	A3	RED/WHITE 3rd	32423
30-0186	5311	A4	RED/WHITE 4th	31967
30-0187	5311	A5	TO3 DRIVER	31966
30-0188	5311	A6	DRIVE CONNECTOR	32424
SUPPORTS:	CDC 9760/9762			
30-0108		SWR + CLOCK	GREEN/YELLOW/GREEN	35605
30-0158		EXTENDED MEMORY CONTROL	GREEN/WHITE	38685
30-0302		BUS TERMINATOR (M9302)		
30-0483	5311	A25		
30-0484	5311	A36		
30-0182	5311	A25		35336
30-0285	5311	A25		
30-0247	5311	A36		31965
30-1024	SH11	16 line DH11		43727
30-1016	"	"		43728
30-1014	"	"		43729
30-1015	"	"		43730

TECH TIPS

SYSTIME QUAD DL

The drawings for this unit specify the TMS 6011 UART, however, one was recently received at MAD fitted with National Semiconductors MM5305 devices. At high baud rates there were no problems with the board, but at low baud rates (i.e. 300 and below) the board failed numerous tests in ZLD on all channels.

This particular UART's response to a "RESET RX DONE" signal is dependent upon the clock frequency. At low frequencies it takes longer for the device to negate RX DONE than it does at higher frequencies. There is, therefore, a conflict at the "RX DONE" stat which is attempting to reset because of the presence of the signal "SELØ:L" (Reading RX Buffer) but is also trying to set because the "R DONE" signal from the UART is slow to negate. As a consequence the stat stays in the same state, i.e. set.

Because the RX DONE status bit is unreliable at low baud rates the following tests fail:-

31 Reading RBUF does not clear RX DONE.
36 Reading RBUF does not clear Interrupt.
43 Data Compare Error.
45 Incorrect Receive Count.

These problems were all cured by fitting UARTs equivalent to TMS 6011 (CFM Bin 17661).

It is also strongly suspected that the above could cause "on line" problems.

N.B. This should not be confused with the failure of ZDLD test 32 on SYSTIME DL's (RDR enable does not clear on Rx done) which is because Systime do not use RDR enable.

SYSTIME DUAL DL11 AS CONSOLE INTERFACE

In Systime systems where a Dual DL11 I/F (Part No. 030-0093) is used as the console device, it must be configured as a Single DL11. This is particularly important in 5000 systems.

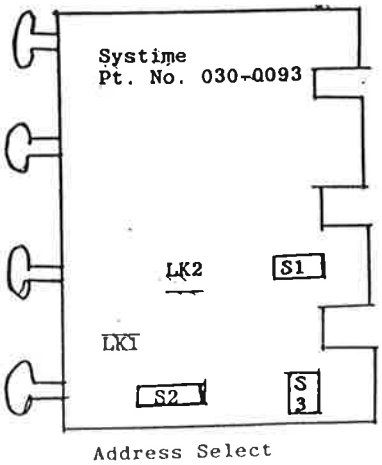
If the second DL11 is linked in, it will be dual-addressed with the switch register and three memory management registers.

When RSTS is running every time user mode is selected (Bits 5. and 6.), Bit 6. will set in the 2nd DL11 output status register, causing an interrupt to 74. RSTS will recover from this error, but the dual addressing will cause other system problems.

The only diagnostic which will show this problem is the memory management basic logic test.

FKTHAØ for 11/34

If the problem is present the program will halt at location 100. The problem could also occur with a faulty DL11.



LK1 - Out = Single DL
LK2 - In

LK1 - In = Dual DL
LK2 - Out

1104 PROCESSOR (M7263)

We have recently had an 1104 Processor PCB from a Systime 1000 site that would not run the DEC Traps Test DGKAB and would not boot using an M9301 Bootstrap.

The cause of this was that the PCB had been modified so that it only caused the forcing of Address Bits A16 and A17 when Bits A12, A13, A14 and A15 were all true, i.e. 170000 forces 770000.

DEC Convention is to force A16 and A17 when Bits A13, A14 and A15 are true. The reason for this is that Systime possibly use the extra 2K of memory.

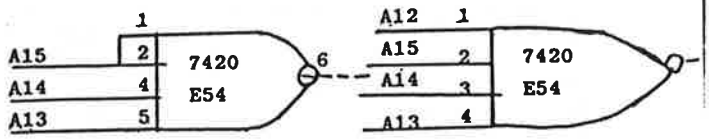
Therefore be warned that:-

a) A "pure" DEC PCB may fail in a Systime Site and
b) A Systime modified PCB will not run on original DEC software or boot using bootstrap/terminator.

UNMODIFIED

MODIFIED

E45/2-

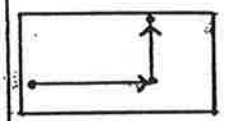


Power on Boot Problems on 11/34 Etc.

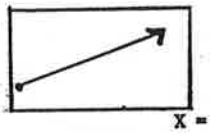
When faced with the problem of intermittent power-on boot failures, the first suspect would usually be the bootstrap, terminator board. Changing this board may seem to cure the problem but it is possible that the fault is not on this board, but on the A.C. power monitor p.c.b. At power up, the supply voltages should come up first followed by the negation of DCLO, then the negation of ACLO which triggers the boot sequence. It is possible for the transistors controlling ACLO and DCLO to fail in an o/c condition. This means that ACLO and DCLO will follow the supply rails at power up, without the necessary delays. In most cases, the boot sequence will still trigger on but on some boards, may be intermittent.

The other main problem with this failure is that the processor will not receive any mains fail indication from the circuit, which could cause unexplained crashes.

It is recommended that the correct action of ACLO and DCLO at power up should be checked if intermittent boot failures are experienced. Triggering a scope to show the signals is not easy and a simple way is to use X - Y mode. To check the delay between 5V coming up and DCLO going false, connect the X input to the +5V and the Y input to the DCLO rail. At switch on the trace shown below should be observed. To check the DCLO to ACLO delay connect X input to DCLO and Y input to ACLO; when the same trace should be seen.



Good Trace



Bad Trace

Set scope to X - Y mod
Input sensitivity to IV/cm

	a	b
X =	+5	DCLO
Y =	DCLO	ACLO

RSTS/E V7 1

RSTS/E V7 1 was officially announced by DEC in January 1982. It is slightly different to previous versions of RSTS/E, in that it uses an optional DCL (Digital Command Language), not unlike the VAX/VMS DCL, and with the same format as RT11 DCL. This, in some sites, will replace the familiar "READY" with a"$" prompt.

The following hardware will be supported on RSTS/E V 7 1 only for systems upgrading from RSTS/E V 7 0 to V7 1. RSTS/E support for these devices will be stopped in October 1983.

Device	Suggested Replacement
RPR ø2	RMø2
RPø3	RMø2
RKø5J (as system disk)	RLø2
RKø5F (as system disk)	RLø2

The RXO2 key-in boot routine is rather long winded to type in using the console (47 instructions). Below is a simple key-in routine which loads the RXO2 registers only:-

```
$ 777170 / 407 <LF>
$ 777172  1<CR>
$ 777172 / 1 <CR>
$ 777170 / 403<LF>
$ 777172  200 <CR>
$ 777172 / 0 <CR>
$ 777172 / 407 <LF>
$ 777172  3 <CR>
$ 777172 / 1 <CR>
$ 777170 / 403 <LF>
$ 777172  200 <CR>
$ 777172  400 <CR>
$ 10 / 0  CR
$ 0G
```

2035	AA	PCB	M	002	MODULE
2036	AA	PCB	M	040	HIGH CURRENT DRIVER
20306	AA	PCB	M	044	SOLENOID DRIVER
12819	AA	PCB	M	050	TU 10 INVERTER DRIVER
8883	AA	PCB	M	100	TU 10 BUS DATA I/F
8888	AA	PCB	M	101	MODULE
8884	AA	PCB	M	102	NEO BUS
8889	AA	PCB	M	103	DEVICE BUS SELECTOR PDP8I
4568	AA	PCB	M	105	TMB11 ADDR SELECTOR
11750	AA	PCB	M	106	BUS RECEIVER
7660	AA	PCB	M	109	PDP11 DEVICE SELECTOR
2034	AA	PCB	M	111	MODULE
8862	AA	PCB	M	112	MODULE
2554	AA	PCB	M	113	MODULE
2555	AA	PCB	M	115	MODULE
8863	AA	PCB	M	116	MODULE
8864	AA	PCB	M	117	MODULE
8575	AA	PCB	M	119	MODULE
2804	AA	PCB	M	121	MODULE
20496	AA	PCB	M	127	MODULE
8866	AA	PCB	M	140	MODULE
8865	AA	PCB	M	141	MODULE
7004	AA	PCB	M	149	MODULE
31666	AA	PCB	M	152	MODULE
12519	AA	PCB	M	160	MODULE
2556	AA	PCB	M	161	BINARY TO OCTAL DE-CODER
8867	AA	PCB	M	163	BINARY TO DECIMAL DECODER
31667	AA	PCB	M	164	6 BIT ADDER PDP 15
31662	AA	PCB	M	169	FUNCTIONAL GATE PDP 12
20497	AA	PCB	M	202	MODULE
8869	AA	PCB	M	203	MODULE
4775	AA	PCB	M	204	MODULE
7005	AA	PCB	M	205	MODULE
8885	AA	PCB	M	206	MODULE
4776	AA	PCB	M	207	MODULE
8870	AA	PCB	M	208	BIT SHIFT&BUFF REG
2557	AA	PCB	M	212	SHIFT REG
8871	AA	PCB	M	214	BIT ACCULALATOR
2558	AA	PCB	M	216	MODULE
33875	AA	PCB	M	217	CLK REG PDP 12
12520	AA	PCB	M	220	REG PDP 8/I
33876	AA	PCB	M	221	MODULE
2541	AA	PCB	M	222	TAPE REG PDP 12
7016	AA	PCB	M	224	DATA PATHS KA11
7017	AA	PCB	M	225	PROCESSOR MEMORY KA11
8887	AA	PCB	M	228	TC08-TC15 TRACK DECODER
20480	AA	PCB	M	233	MODULE
8916	AA	PCB	M	234	MODULE
8872	AA	PCB	M	236	MODULE
8873	AA	PCB	M	238	MODULE
8874	AA	PCB	M	239	MODULE
8576	AA	PCB	M	302	MODULE
8875	AA	PCB	M	304	MOUDLE
7008	AA	PCB	M	306	MODULE
8876	AA	PCB	M	307	MODULE
12521	AA	PCB	M	310	TAPED DELAY LINE
7009	AA	PCB	M	311	DUAL TAPED DELAY LINE
31668	AA	PCB	M	312	MODULE
1791	AA	PCB	M	360	VARIABLE DELAY LINE
2559	AA	PCB	M	401	VARIABLE CLOCK
2563	AA	PCB	M	405	RK11-C CRYSTAL CLK
18049	AA	PCB	M	410	MODULE

```
31675 AA  PCB M 420 RP09-RP15-PHASE LOCK CLK
 2809 AA  PCB M 452 TELETYPE CLOCK
38171 AA  PCB M 454
11754 AA  PCB M 500 NEG BUS RECEIVER
12820 AA  PCB M 502 NEG INPUT CONVERTER
 2808 AA  PCB M 503 MODULE
 2038 AA  PCB M 506 MODULE
31669 AA  PCB M 510 I/O BUS RECEIVER
20644 AA  PCB M 514 TU10 TRANSCEIVER
12522 AA  PCB M 516 MODULE
18059 AA  PCB M 517 MODULE
 7383 AA  PCB M 518 MODULE
 8901 AA  PCB M 531  8 CHAN NEG BUS RECEIVER
 7012 AA  PCB M 594 DF11-A                    P
 7136 AA  PCB M 598 DF11-K
 4777 AA  PCB M 602 MODULE
20483 AA  PCB M 604 MODULE
20498 AA  PCB M 606 PULSE AMPLIFIER
 8877 AA  PCB M 611 DB11-A HIGH SPD PWR INVTRP
 2805 AA  PCB M 617 MODULE
31672 AA  PCB M 622 MODULE
 2033 AA  PCB M 623 RK11-C BUS DRIVER
20482 AA  PCB M 624 MODULE
 4778 AA  PCB M 627 TM11-TMA11 PWR AMPLIFIER
11755 AA  PCB M 632 MODULE
 8886 AA  PCB M 633 MODULE
20654 AA  PCB M 640 TU10 MSTR/I/F BUS DRIVER
 2039 AA  PCB M 650 NEG OUTPUT CONVERTER
18060 AA  PCB M 651 MODULE
12523 AA  PCB M 660 POS LEVEL DRIVER PDP8/1
18072 AA  PCB M 661 MODULE
31665 AA  PCB M 688 TM11-TMA11 UNIBUS PWR
12524 AA  PCB M 700 FAIL DRIVERS
18074 AA  PCB M 702 MODULE
 2806 AA  PCB M 706 ASYCH LINE RECEIVER
 2807 AA  PCB M 707 MODULE
19190 AA  PCB M 710 PUNCH CTL PDP 8/I
 2560 AA  PCB M 711 SCOPE CTL PDP 12
19192 AA  PCB M 715 READER CLK
 2564 AA  PCB M 719 KW12 CLK SYNCH DECOD CONV
 2561 AA  PCB M 720 NON-EXIST MEM DETECTOR
 4553 AA  PCB M 721 KA11 BUS I/F 1
 7018 AA  PCB M 724 KA11 BUS&CONSOLE CTL
 7019 AA  PCB M 725 KA11 BUS I/F
 7020 AA  PCB M 726 KA11 I/R DECODER
 7021 AA  PCB M 727 KA11 STATE CTL
31421 AA  PCB M 727YA KA11 STATE CTL
 7022 AA  PCB M 728 KA11 TIMING&STATES
 7061 CC  PCB M 729 MM11-E CTL LOG TIMING
 7661 AA  PCB M 729 MODULE
18051 AA  PCB M 750 MODULE
18052 AA  PCB M 751 DC08 LINE REG
```

34476	AA	PCB M7822 DU11
20394	AA	PCB M7846 RX11- UNI CTL
24199	AA	PCB M7847 MEM-K 11/04
37972	AA	PCB M7847-YJ MOS MEM MS11JP
23219	AA	PCB M7850 PARITY
39551	AA	PCB M7854 MODULE
990485	AM	PCB M7855 UNIBUS EXERCISER
20693	AA	PCB M7856 MODULE
31162	AA	PCB M7859 INTERFACE FOR KY11B
38953	AA	PCB M7860 (DR11-C)
26979	AA	PCB M7867 DUP11
31212	AA	PCB M7891-BA MS11-LB 128KB MEM
20500	AA	PCB M7892 MODULE
28490	AA	PCB M7900 MODULE
28498	AA	PCB M7901 MODULE
28499	AA	PCB M7902 TMB11
28500	AA	PCB M7903 MODULE
28501	AA	PCB M7904 MODULE
35131	AA	PCB M7906 SERVO ANALOG
35129	AA	PCB M7907 SERVO CONTROL
35130	AA	PCB M7908 TRACK POSITION OSC
33498	AA	PCB M7910 MODULE
31568	AA	PCB M7911 TMB11-I/F
31569	AA	PCB M7912 TMB11 UNI REG
32292	AA	PCB M7930 MODULE DEC CP-11
20721	AA	PCB M7940 DLV11-
35526	AA	PCB M7941 MODULE (DRV11)
39402	AA	PCB M7942 (MRV11)
23221	AA	PCB M7944 (MSV11-B 8KB MEM)
28658	AA	PCB M7944 MSV11-B
20396	AA	PCB M7946 RXU11-A
39684	AA	PCB M7952 (KWV11-A)
39682	AA	PCB M7954 (IBV11-A)
28053	AA	PCB M7955-YD (MSV11-CD)
39902	AA	PCB M7955-YJ (MSV11-C)
39046	AA	PCB M7957
38591	AA	PCB M7982
28051	AA	PCB M8012 YA BDV11-
28054	AA	PCB M8013 RLV 11 OPT
28055	AA	PCB M8014 RLV 11 OPT
38752	AA	PCB M8017 MODULE (DLV11-EB)
39576	AA	PCB M8021 (MRV11-BA)
28059	AA	PCB M8028 DLV 11-F
33007	AA	PCB M8029 RXV 211
28058	AA	PCB M8043 DLV11-J
34045	AA	PCB M8044 DB MSV 11-D
34047	AA	PCB M8047 CA MXV11-4 MULTIFUNCTION
30190	AA	PCB M8100 KB11A GEN REG&CTL 11/45
30193	AA	PCB M8101 11/45
30195	AA	PCB M8102 KB11A INSTRU REG&DECODE
30200	AA	PCB M8103 KB11A ROM&ROM CTL
30199	AA	PCB M8104 KB11A PROCE DATA&UNI REG

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 30226 AA   PCB M8105 KB11A TRAP&MISCELLAN CTL
 30227 AA   PCB M8106 KB11A UNI&CONSOLE CTL
 31392 AA   PCB M8107 KT11C SYSTEM ADDR PATH
 31393 AA   PCB M8108 KT11C SYSTEM STAT REG
 30219 AA   PCB M8109 KB11A TIMING GENERATOR
 30218 AA   PCB M8116 KB11A SYSTEM JUMPER
 35184 AA   PCB M8126 MODULE
 35185 AA   PCB M8127 MODULE
 35186 AA   PCB M8128 MODULE
 35187 AA   PCB M8129 MODULE
 34046 AA   PCB M8186 KD11 LS11/23
 31190 AA   PCB M8200-YB MODULE (DMC11-AL)
 38047 AA   PCB M8202-YA
 34603 AA   PCB M8256 MODULE
 24059 AA   PCB M8264
 27617 AA   PCB M8265 DATA PATHS (11/34A)          F
 27618 AA   PCB M8266 CONTROL (11/34A)             F
 27317 AA   PCB M8267 MODULE  FP11A FLOATING PT
 31402 AA   PCB M8268 MODULE
 35192 AA   PCB M8290 CR11-CM11 I/F
 21568 AA   PCB M8293 MF11-U
 30298 AA   PCB M8294 MODULE
 31349 AA   PCB M8295 C.S.S. MODULE
  7371 AA   PCB M8300 REG CTL PDP 8
  7372 AA   PCB M8310 REG CTL PDP 8
  7359 AA   PCB M8320 BUS LOAD PDP 8E
 20218 AA   PCB M8329 PARRALL I/F LA30
  7373 AA   PCB M8330 TIMING GENERATOR PDP8
 20219 AA   PCB M8331 TA 8/E CTL
  7386 AA   PCB M8340 EAE INSTRUC CTL
  7387 AA   PCB M8341 EAE REG CTL
 21622 AA   PCB M8350 FAST POSIT BUS IF PDP8E
 38737 AA   PCB M8360 MODULE
  7388 AA   PCB M8650 DL8E 150 BAUD
 20221 AA   PCB M8655 KL 80
 37891 AA   PCB M8722 MS11MB MEMORY 256KB E.C.C
 31983 AA   PCB M8901 TU16 DATA SYNCHRONIZER
 31984 AA   PCB M8902 TM02 TAPE CTL P.E.
 31985 AA   PCB M8904 TM02 TAPE CTL NRZ1
 31986 AA   PCB M8905 TM02 MAINTEN REG
 31987 AA   PCB M8906 TM02 16 BIT FIDDLER
 31988 AA   PCB M8907 MODULE
 31989 AA   PCB M8908 MODULE
 31990 AA   PCB M8908-YA MODULE
 31991 AA   PCB M8909 TM02 MASS BUS I/F
 31994 AA   PCB M8910 TU16 LOG&WRITE
 31995 AA   PCB M8911 TU16 SLAV CLK MOTN DELAY
 31996 AA   PCB M8912 MODULE
 32001 AA   PCB M8913-YA MODULE
 30860 AA   PCB M8916 MODULE
 31570 AA   PCB M8920 TS03 TU10 MSTR BUS I/F
 38588 AA   PCB M8922
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18053 AA   PCB M 752 INSTRUCTION DECODER
18058 AA   PCB M 753 MODULE
 2562 AA   PCB M 760 A/D CTL PDP 12
20645 AA   PCB M 763 TU10 9 TRACK WRITE BUFF
20646 AA   PCB M 765 TU10 9 TRACK READ BUFF
20647 AA   PCB M 767 TU10 CLK&SKEW DELAY
20648 AA   PCB M 768 TU10 DELAY SELECTOR
20649 AA   PCB M 769 TU10 FUNCTIONAL CTL
31200 AA   PCB M 780 TRANS/REC FOR KL11
20309 AA   PCB M 781 PC11 CTL FOR KA11
 4569 AA   PCB M 782 INTERUPT CTL
11756 AA   PCB M 783 DB11-A DRIVER
 8879 AA   PCB M 784 DB11-A RECEIVER
29835 AA   PCB M 785 DB11-A TRASCEIVER 4 PER
 4570 AA   PCB M 786 MODULE
21567 AA   PCB M 787 KW11-C L.T.C.                    P
31210 AA   PCB M 792 DISC LOADER ROM
 7087 AA   PCB M 792 MODULE                          P
38169 AA   PCB M 794 MODULE
 7010 AA   PCB M 795 TMB11 WRD COUNT&BUS ADDR
 7011 AA   PCB M 796 TMB11 UNIBUS MSTR CTL
 8577 AA   PCB M 797 MODULE
 8578 AA   PCB M 798 UNIBUS DRIVER
18073 AA   PCB M 805 MODULE
 7023 AA   PCB M 820 KA11 DATA PATH CTL 11/20
 7024 AA   PCB M 821 KA11 MEM CTL 11/20
 7025 AA   PCB M 822 KA11 FLAG CTL 11/20
 7026 AA   PCB M 823 CODES DATA 11/20
 7027 AA   PCB M 824 KA11 PRIORITY 11/20
 7028 AA   PCB M 825 PWR FAIL 11/20
 8914 AA   PCB M 827 KF11-A CLK&STATES
 7370 AA   PCB M 835 POSITIVE BUS I/F PDP 8E
 7384 AA   PCB M 837 MEM EXTEN CTL PDP 8E
34458 AA   PCB M 847E
20217 AA   PCB M 848 PWR FAIL DETC&AUT REST 8E
 7369 AA   PCB M 849 FRI SHIELD 8-E
 7382 AA   PCB M 860 R.T.C.
31026 AA   PCB M 873 UNIBUS REST
31404 AA   PCB M 873B MODULE (KW11L)
38736 AA   PCB M 883 MODULE
20650 AA   PCB M 890 TU10 MOTION CTL
20631 AA   PCB M 891 TU10 CRC&WRITE GATING
20638 AA   PCB M 892 TU10 GAD TIMING&RD PARITY
20632 AA   PCB M 893 TU10 9 TRACK WRITE BUFF
20656 AA   PCB M 896 TU10 CRCC CHECKER
18075 AA   PCB M 900 MODULE
31417 AA   PCB M 904  MODULE W/CABLE
 2032 AA   PCB M 906 CABLE TERMINATOR
 2031 AA   PCB M 907 MODULE
12821 AA   PCB M 908 MODULE
31671 AA   PCB M 911 TERMINATOR
18204 AA   PCB M 919B MODULE
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11758 AA  PCB M 920 DB11-A BUS CONNECTOR 2PER
23520 AA  PCB M 930 DB11A BOS TERMINATOR 2PER
38738 AA  PCB M 935 BACKPLANE JUMPER
31416 AA  PCB M 941A MODULE
29315 AA  PCB M 957 MODULE                                  P
38170 AA  PCB M 970 MODULE
33243 AA  PCB M 972 MODULE
31318 AA  PCB M 973 MODULE
33242 AA  PCB M 974 DB11 MAINTENANCE JUMPER
31203 AA  PCB M 981 MODULE
31211 AA  PCB M 983 MODULE
32929 AA  PCB M S AMPLIFIER
32927 AA  PCB M S READ CHECK
 4576 AA  PCB M1091 MEMORY DEVICE SELECT MODULE
31664 AA  PCB M1103 MODULE
31663 AA  PCB M2500 MODULE
29314 AA  PCB M4050 CRYSTAL CLK
25311 AA  PCB M4540 MODULE
25163 AA  PCB M5900 DS11-RECEIVER
25161 AA  PCB M5901 DS11-TRANSMITTER
25168 AA  PCB M5902 DS11 TRANSCEIVER
31992 AA  PCB M5903-YA BUS TERMINATOR
31980 AA  PCB M5904 MAS BUS CTL TRANSCEIVER
25146 AA  PCB M5942 MODULE
30892 AA  PCB M7011 UART SERIAL I/F
30891 AA  PCB M7013 VT40 VECTOR&CHAR GENERAT
31582 AA  PCB M7014-YA-1 MODULE
32921 AA  PCB M7024 VT55 GRAPHICS CTL                       )
19191 AA  PCB M7050 MODULE
 7013 AA  PCB M7065 SYNCH LINE RECEIVER
 7014 AA  PCB M7075 SYNCH LINE TRANSMITTER
32185 AA  PCB M7081 MODULE
37688 AA  PCB M7090 CONSOLE INT. MODULE
38950 AA  PCB M7093 (FP11-F)
37689 AA  PCB M7094 DATA PATHS
37675 AA  PCB M7095
37690 AA  PCB M7096 MULTIFUNCTION MODULE
37691 AA  PCB M7097 CACHE MEMORY
37692 AA  PCB M7098 UNIBUS INT. MODULE
33999 AA  PCB M7104 RK8-E DATA BUFF&STATUS
34000 AA  PCB M7105 RK8-E MAJOR REG
34001 AA  PCB M7106 RK8-E CTL
31348 AA  PCB M7114 MODULE (VT30H)
39643 AA  PCB M7133 PROCESSOR
39648 AA  PCB M7134 UNIBUS MAP OPTION
 8917 CL  PCB M7210 KE11-DATA CTL
 8915 AA  PCB M7211 KE11-A REG CTL
29834 AA  PCB M7212 DB11-A ADDR BUFF
29832 AA  PCB M7213 DB11-A BUFF MSTR
 4550 AA  PCB M7216 PRIORITY PLUS CONTROL MODULE
 4562 AA  PCB M7217 POWER FAIL MODULE
20477 AA  PCB M7219 RC11 BUS I/F                            P
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7015	AA	PCB M7223 DP11-AA CTL	
7658	AA	PCB M7228 KW11-P R.T.C PROGAMABLE	
8940	AA	PCB M7231 DATA PATHS KD11-A 11/40	P P
8941	AA	PCB M7232 U WORD KD11-A 11/40	P
8937	AA	PCB M7233 IR DECODE KD11-A 11/40	P
8938	AA	PCB M7234 IMING KD11-A 11/40	P
8939	AA	PCB M7235 STAT PROCESS KD11A 11/40	PP
31205	AA	PCB M7236 MEM MAN-MENT KD11A 11/40	
21565	AA	PCB M7237 STACK LIMIT REG 11/40	
31300	AA	PCB M7238 MODULE (KE11-E)	
31207	AA	PCB M7239 KE11-F E.I.S.	
25178	AA	PCB M7240 DM11-A CTL	
25179	AA	PCB M7241 DM11-B CTL	
25180	AA	PCB M7242 DM11-C CTL	
25183	AA	PCB M7243 DM11 TRANSMITTER	
25184	AA	PCB M7244 DM11 TRANSMITTER	
25185	AA	PCB M7245 DM11 TRANSCEIVER	
29833	AA	PCB M7248 DB11A UNIBUS REPEATER	
27319	AA	PCB M7251 MODULE	
20762	AA	PCB M7254 RK11D STAT CTL	
20763	AA	PCB M7255 RK11D DISC CTL	
20764	AA	PCB M7256 RK11D DATA PATHS	
20765	AA	PCB M7257 RK11D BUS CTL	
31031	AA	PCB M7258 PARRALL I/F	
21566	AA	PCB M7259 MF11-LP PARITY	
20671	AA	PCB M7260 DATA PATH KD11-B 11/05	
20672	AA	PCB M7261 CTL LOG&PROG DD11B 11/05	
27390	AA	PCB M7263 KD11-D PROCESSOR 11/04	P
20719	AA	PCB M7264 DK11-F LSI 11-CPU 4K RAM	
28049	AA	PCB M7264-YC MODULE	P
24058	AA	PCB M7265	
24057	AA	PCB M7266	
30653	AA	PCB M7270 KD11-HA LSI-11/2	
25307	AA	PCB M7277 DH11- SCANNER	
25308	AA	PCB M7278 DH11- REG&BYTE COUNT	
25155	AA	PCB M7279 DH11- DJ11 IF IO	
25154	AA	PCB M7280 DJ11-8 UHARTS	
25167	AA	PCB M7285 DJ11- MUX CTL	
25309	AA	PCB M7288 DH11- LINE PARAMETER CTL	
25310	AA	PCB M7289 DH11- RECEIVER SCANNER	
4580	AA	PCB M7290 CONTROL MODULE	
30315	AA	PCB M7293 MM11/UP TIMING & CTL I/F	
31978	AA	PCB M7294 RH11 DATA BUFF&CTL	
31977	AA	PCB M7295 RH11-A BUS CTL	
31976	AA	PCB M7296 RH11 CTL&STAT REG	
31975	AA	PCB M7297 RH11 MASS BUS PARITY CTL	
7135	AA	PCB M7389 MODULE	
25578	AA	PCB M7390 MODULE (LP11 INTERFACE)	
32008	AA	PCB M7395 RT02 DISPLAY CTL	
32007	AA	PCB M7399 RT02 AUDIO ALARM	
30308	AA	PCB M7410 MODULE	
30309	AA	PCB M7417 MODULE	

36332	AA	PCB M7592
20651	AA	PCB M7670 TU10 FORWARD TIMER
20655	AA	PCB M7671 TU10 MSTR-SLAV BUS DRIVE
20630	AA	PCB M7672 TU10 MSTR CTL BUFF
20633	AA	PCB M7673 TU10 DATA CHECKER
30725	AA	PCB M7680 MODULE
30726	AA	PCB M7681 MODULE
7106	AA	PCB M7700 RK05 INDEX SECTOR
7103	AA	PCB M7701 RK05 CTL-INTERLOCK
7109	AA	PCB M7702 RK05 TRACK ADDR DIFFER
30088	AA	PCB M7705 MODULE
30089	AA	PCB M7706 MODULE
30090	AA	PCB M7707 MODULE
30091	AA	PCB M7708 MODULE
7091	AA	PCB M7710 LA 30 PRINT CYCLE&TIMING
7090	AA	PCB M7711 LA 30 CTL LOG A
7088	AA	PCB M7712 LA 30 CTL LOG B
7097	AA	PCB M7713 LA30 RIB CTL&LT CHA VISI
7092	AA	PCB M7714 LA30 CHARA GENERATOR
7093	AA	PCB M7715 LA30 LINE FEED CTL
7094	AA	PCB M7716 LA30 MOTOR TRANSLATOR
7095	AA	PCB M7717 LA30 MOTOR CTL
7096	AA	PCB M7720 MODULE
31319	AA	PCB M7721 LA36 CTL LOG IC A
20770	AA	PCB M7722 LA36 MICRO PROCESSOR
20771	AA	PCB M7724 LA36 MICRO PROCESSOR
7098	AA	PCB M7724 MODULE
20333	AA	PCB M7726 RX01 FLOPPY CTL
20334	AA	PCB M7727 RX01 R/W CTL
20772	AA	PCB M7728 MODULE
30092	AA	PCB M7729 MODULE
30093	AA	PCB M7730 MODULE
7134	AA	PCB M7731 LA30 SERIAL I/F
33008	AA	PCB M7744 RX02 FLOPPY DISC CTL
33009	AA	PCB M7745 RX02 R/W CTL
20502	AA	PCB M7760 TU60 LOG
20501	AA	PCB M7761 TU60 SERVO&READ
31196	AA	PCB M7762 DISC CONTLER
8942	AA	PCB M7800 KL11
20690	AA	PCB M7800-0-1 MODULE
20691	AA	PCB M7800-YA-1 MODULE
35193	AA	PCB M7807 MODULE
32781	AA	PCB M7810 READER PUNCH CONTROL
28340	AA	PCB M7812 DQ11-AA BUS SELECTOR
28342	AA	PCB M7813 DQ11AA CHAR CNT BUS ADDRP
28341	AA	PCB M7815 DQ11 AA MODEM CTL
29311	AA	PCB M7816 DQ11AB CHA DETC&SEQ CNT
29310	AA	PCB M7817 MODULE
28343	AA	PCB M7818 DQ11 AA CAR DETC
26943	AA	PCB M7819 DZ11-A
20310	AA	PCB M7820 INTERUPT CTL
8878	AA	PCB M7821 TMB11- INTERUPT CTL

38580	AA	PCB M8923
38581	AA	PCB M8924
30888	AA	PCB M8926 MODULE
38584	AA	PCB M8929
38589	AA	PCB M8962
38583	AA	PCB M8963
38582	AA	PCB M8964
38587	AA	PCB M8965
38585	AA	PCB M8966
38586	AA	PCB M8967
38590	AA	PCB M8968
32000	AA	PCB M9001-YB MODULE
32002	AA	PCB M9001-YC MODULE
31328	AA	PCB M9016 MODULE
31624	AA	PCB M9200
30822	AA	PCB M9202 KD11-2
31979	AA	PCB M9300 UNI TERMINATOR B
23216	AA	PCB M9301 BOOT TERMINATOR 11/23
33992	AA	PCB M9301 YB MODULE
31311	AA	PCB M9301-YA MODULE
27621	AA	PCB M9301-YF MODULE BOOT/TERM/EMULR
23215	AA	PCB M9302 MODULE BUS TERMINATOR
31165	AA	PCB M9312 MODULE BOOT/TERMINATOR
23222	AA	PCB M9400 YA BOOT TERM 11/23
31424	AA	PCB M9400-YC MODULE
27356	AA	PCB M9400YA MODULE
31321	AA	PCB M9630 MODULE
28402	AA	PCB M9680A MODULE
31188	AA	PCB M9700 WITH CABLE (DQ11)
29316	AA	PCB M9760 MODULE
32784	AA	PCB M9970

20636	AA	PCB G 062 MODULE
20637	AA	PCB G 064 MODULE
30867	AA	PCB G 066 MODULE
2394	AA	PCB G 083 MODULE
4997	AA	PCB G 085 MODULE
4574	AA	PCB G 102 MODULE
4575	AA	PCB G 103 MODULE
7368	AA	PCB G 104 MODULE
7385	AA	PCB G 105 MODULE
7000	AA	PCB G 110 MODULE
26318	AA	PCB G 111 MODULE
21563	AA	PCB G 114 MODULE
30296	AA	PCB G 116 MODULE
7108	AA	PCB G 180 MODULE
1879	AA	PCB G 208 MODULE
1880	AA	PCB G 209 MODULE
12516	AA	PCB G 221 MODULE
4577	AA	PCB G 225 MODULE
7366	AA	PCB G 227 MODULE
2550	AA	PCB G 228 MODULE
4999	AA	PCB G 231 MODULE
26319	AA	PCB G 233 MODULE
31169	AA	PCB G 234 MODULE
21564	AA	PCB G 235 MODULE
30297	AA	PCB G 236 MODULE
4578	AA	PCB G 266 MODULE
18240	AA	PCB G 284 MODULE
11744	AA	PCB G 285 MODULE
11745	AA	PCB G 286 MODULE
4998	AA	PCB G 290 MODULE
20478	AA	PCB G 294 MODULE
20479	CC	PCB G 295 MODULE
20485	AA	PCB G 296 MODULE
20639	AA	PCB G 350 MODULE
7085	AA	PCB G 380 MODULE
7100	AA	PCB G 381 MODULE
18218	AA	PCB G 603 MODULE
4579	AA	PCB G 616 MODULE
12517	AA	PCB G 624 MODULE
30317	AA	PCB G 647 MODULE
33509	AA	PCB G 651 MODULE
20720	AA	PCB G 655 MODULE
20481	AA	PCB G 680 MODULE
31647	AA	PCB G 711 MODULE
20768	AA	PCB G 712 MODULE
33942	AA	PCB G 718 MODULE
33873	AA	PCB G 719 MODULE
11748	AA	PCB G 723 MODULE
7001	AA	PCB G 736 MODULE
7002	AA	PCB G 740 MODULE
20653	AA	PCB G 741 MODULE
34370	AA	PCB G 741 YA
8904	AA	PCB G 742 MODULE
31425	AA	PCB G 772A MODULE
29317	AA	PCB G 772B MODULE
11749	AA	PCB G 775 MODULE
12518	AA	PCB G 785 MODULE
1881	AA	PCB G 802 MODULE
2391	AA	PCB G 805 MODULE
1882	AA	PCB G 808 MODULE
18201	AA	PCB G 809 MODULE
31674	AA	PCB G 820 MODULE
12818	AA	PCB G 821 MODULE
2393	AA	PCB G 824 MODULE
2551	AA	PCB G 826 MODULE
25340	AA	PCB G 836 MODULE
25341	AA	PCB G 840 MODULE
8903	AA	PCB G 847 MODULE
8902	AA	PCB G 848 MODULE
7649	AA	PCB G 850 MODULE
2552	AA	PCB G 851 MODULE
1883	AA	PCB G 852 MODULE
33941	AA	PCB G 853 MODULE
18062	AA	PCB G 856 MODULE
8905	AA	PCB G 859 MODULE
18066	AA	PCB G 861 MODULE
18067	AA	PCB G 862 MODULE
12339	AA	PCB G 879 MODULE
2553	AA	PCB G 882 MODULE
8882	AA	PCB G 888 MODULE
33874	AA	PCB G 906 MODULE
2392	AA	PCB G 916 MODULE
2037	AA	PCB G 918 MODULE
20640	AA	PCB G 932 MODULE
20641	AA	PCB G 933 MODULE
31320	AA	PCB G 936 MODULE
7104	AA	PCB G 938 MODULE
30727	AA	PCB G 938 YA MODUL
38579	AA	PCB G157
39650	CC	PCB G7273 GBANI C(
38172	AA	PCB G8000A FILTER

31195	AA	PCB H 205 MODULE (DR11B)
31420	AA	PCB H 207 MODULE
26320	AA	PCB H 212 MODULE
20669	AA	PCB H 213 MODULE 4K X 16K
20670	AA	PCB H 214 MODULE 8K X 16K
30310	AA	PCB H 215 MODULE
21569	AA	PCB H 217 MODULE
31625	AA	PCB H 217C MODULE
7367	AA	PCB H 220 MEMORY STACK
24193	AA	PCB H 222 MODULE
30299	AA	PCB H 224 32K STACK
20688	AA	PCB H 400 MODULE
20652	AA	PCB H 603 MODULE
7105	AA	PCB H 604 MODULE
7086	AA	PCB H 605 MODULE
31997	AA	PCB H 606 MODULE
31982	AA	PCB H 870 MODULE
31818	AA	PCB H1415 LINE DRIVER/RECEIVER
3149)	AA	PCB H7831 MODULE

CABLE LISTING BY EQUIPMENT

WHERE USED	CABLE MODEL NO.
AA15	BC01P
	BC01R
D11K	BC20F
AD15	BC01P
	BC01R
GL2	BCLA2
M11K	BC20H
	BC11T
AN10	BC10T
N20	BC10T
011	BC11L
ASR33/35	BC04S
	BC04T
	BC04U
	BC04W
	70-05676
	70-06593
	70-07135
A12	BC90C
A903/4/5	BC95M
	BC95T
DLV11-J (Cont.)	BC21D
	BC24A
	BC24B
	BC24C
DL11A	70-08360
DL11C	70-08360
DL11	BC99J
DMC8E	BC14E
DMC11FA	BC05Z
DMC11M	BC03N
DMP11	BC55M
	BC55N
DMS11	BC11W
	BC11X
DN	BC20R
DN11	BC99K
	BC99R
DPM01	BC41B
	BC41C
DP01A	BC99A
	BC99B
DP8E	BC99L
DP8EA	BC05C
DP8EB	BC01W
DP11	BC99H
DQ11	BC01W
DR8E	BC08S
DRV11-BC04Z, BC07D, BC08R, BC11V	
Interface Kits	BC04Z
KA8E	BC14H
KC341	BC05W
KL8	BC05M
	BC08T
	BC08W
	BC08X
	BC08Y
	BC08Z
	BC14J
KL10	BC20C
KPV11	70-08612, 70-12754
KSR33/35	BC04R
LAP02	BC03M
	BC05D
	BC22A
	BC22B
LAS12	BC22C
LA30	BC05F
	70-08417
LA34	BC21F
	BC21H
	BC21J
	BC22A
	BC22B
	BC23A
	BC23B
LSPVC	BC05N
LS8	70-08859
LS11	70-09087
LT33	70-06594
MASSBUS	BC06R
	BC06S
	BC06V
	BC07A
	BC07B
	BC07C
	BC07D
	BC07K
	BC07L
MA20	BC20C
MF11	70-09565
MG10	BC20D
MNCFT	BC21K
MNC11	BC21C
M7142	BC21S
	BC21T
	BC21U
	BC21V
	BC21W
	BC21X
	BC21Y
M7941	BC05W

WHERE USED	CABLE MODEL NO.
CD11	70-08764, 70-08738
CR8	70-08737, 70-08594
	70-07774, 70-11217
	70-08737, 70-08738
CSC8	BC03V
CSC11	BC03V
DAF11	70-09563
DATEL	BC99M
DA28	BC01Z
DA14E	BC14H, BC14K
DA14L	BC14L
DC02	BC01A, BC01J
DC04-CN, CP	BC01N, BC99T
DC06	BC01C, BC01E
DC08B	74-05151, BC01B
DC08C	BC99A
DC08F	70-05469, BC10V
DC08LD	
DC10	
DRV11-B	BC04Z, BC07D, BC08R
DRV11-J	BC05W, BC11J
DR11A	BC11K, 70-08883
DR11C	BC11J, BC11M
DR11F	BC04Z, BC08R
DR11K	BC04Z, BC08R
DR11L	BC99G, BC05C
DR11M	BC05C, 70-09136
DS10	BC11F, BC03W
DS11	BC02C, BC99S
DS520	BC99V, BC09B
DT11M	BC09B, BC10Z
DT90	BC11U, BC03P
DUP11	BC05D, BC02E
DU11	BC02F, BC02H
DV11	BC02J, BC02K
DW09A	BC02L, BC02M
DW09B	
DX20	
DZV11A	
DZ11	
EIA Ext. Cord	
FPP8A	
LA36	BC02Y, BC02Z, BC03A, BC03B, BC03C, BC03D, BC03E, BC03F, BC03H, BC03J, BC03X, BC03Y, BC20E, BC98A
LA38	BC21F, BC21H
LA120	BC22A, BC22B, BC23A, BC23B
LA180	BC11S, BC80A, BC80H
LC11	70-08417
LE8	70-06964
LK02	BC21T, BC21U
NCV11	BC21E
PA63	BC01F, BC01H, BC20K, BC20P
PCL11B	BC08F
PC11	BC70A, BC70B, BC70C
PDM70	BC01A, BC01C, BC01J, BC01V, BC03L, BC03M, BC04R, BC04S, BC05H, BC05J, BC08A, BC08B, BC08C, BC08D, BC08E, BC08H, BC08J, BC08K, BC08L
PDP-8	

WHERE USED	CABLE MODEL NO.
DC10B	BC01X, BC01Y
DC10E	BC01X, BC01Y
DC11	BC99A, BC99J
DC14	BC14D
DC11D	BC01S
DD01	BC40C, BC41A
DD02	BC40C, BC41A
DDV11-B	70-12754
DD11A	70-09562
DD11B	70-09563, 70-10117, 70-09099
DF10	BC10P
DF11A	BC05F
DF11BA, BB	BC11E
DF11K	BC05F
DJ11	BC99N
DKC8A	BC80A
DK8EA	70-07128
DLV11-J	BC20K, BC20M, BC20N, BC21A, BC21B
FPP8A (Cont.)	BC02N, BC02P, BC02S, BC02T, BC02U, BC02W, BC02X
H304	BCL2B
H305	BCL2A, BCL2B
H332	BC40A, BC40B, BC40L
H912	BC14F
H7004C	BC06L
H7004B	BC06K
IBV11	BN11A
ICSX	BC40H, BC40J, BC40K
ICS8	BC40H, BC40J, BC40K
ICS11	BC40H, BN40A, BN40B, BC40H, BC40J, BC40K
LPC01	BC06J
LPC8	BC06A, BC06B, BC06C, BC06D, BC06E, BC06F
LPC11	BC06A, BC06B, BC06C, BC06D, BC06E, BC06F
LPD8	BC06J
LPD11	BC06J
LPP01	BC03R
LPSVC	BC05P, BC05R, BC05S
LP08	70-08755
LP11	70-11212, 70-06824, 70-08837
LQP01	BC80F
LSI11	BCV1A, BCV1B, BCV1D
PDP-8 (Cont.)	BC08M, BC08N, BC08P, BC08R, BC14B, BC14K, BC20A, BC20B, BC80C, BC99F
PDP-9	70-05313, BC09A, BC09B, BC09C
PDP-10	BC10A, BC10B, BC10C, BC10D, BC10E, BC10H, BC10J, BC10K, BC10L
PDP-11	BC03L, BC03M, BC04R, BC04S, BC05H

WHERE USED	CABLE MODEL NO.
VT78	BC80D, BC80E, BC80F, BC80H
VT100	BC22A, BC22B, BC23A, BC23B
6801	70-06121
14/30	BC14M
VT11	70-09449
VT20	BC05V, BC06T, BC06U
VT50	BN50A, BN50B, BN50C, BC98A
VT52	BN52A, BN52B, BN52C
VT61	BN61C
VT62	BC03Z
VT71	BC03S, BC03T
PDP-15	BC09C, BC09E, 70-06414
PP67	BC01F
PR68D	70-06557
PT08	BC99A, BC99B, 70-05676
RH10	BC10P
RK05	BC01S
RK06	70-12292
RL01/02	70-12122, BC80J
RP01	BC01D
RP02/03	BC01D
RP04/05/06	70-06465, BC06R, BC06S
RP10	70-06463
RTC11	BC20T
RT02	70-08519
RX01/02	BC05L
RX78P	BC80D, BC80E
Tempest	BC20S, BC20U, BC21L
PDP-11 (Cont.)	BC05J, BC05T, BC05U, BC11A, BC11B, BC11C, BC11D, BC11N, BC11P, BC11R, BC44A, BC44B, BC44C, BC44D, BC99D, BCV1C, 70-08288, 70-08820, 70-08855, 70-08864, 70-08909, 70-09087, 70-09205, 70-09206, 70-09242, 70-14060, 70-14090

WHERE USED	CABLE MODEL NO.
MANY USES	BC01V, BC05W, 70-05820, 70-07036, 70-07222, 74-05552, 74-05553, 74-12827
TU10	BC08N, BC08P
TU20	70-05541
TU55	74-05151, BC04X, BC05A
TU56	BC04X, BC04Y, BC05A, BC05B
TU58	BC20Y, BC20Z
TU60	BC05L
TX02	BC10X, BC10Y
TX05	BC10W
UDC	BC40D
VC8E	BC01L, BC01M, 70-08499, 70-08977
VK100	BC26B
VT1XXAH	BC20R
VT05	BC10U, BC99P
VT8E	70-08977, 70-09042
PDP-15	BC09C, BC09E, 70-06414
PP67	BC01F
PR68D	70-06557
PT08	BC99A, BC99B, 70-05676
RH10	BC10P
RK05	BC01S
RK06	70-12292
RL01/02	70-12122, BC80J
RP01	BC01D
RP02/03	BC01D
RP04/05/06	70-06465, BC06R, BC06S
RP10	70-06463
RTC11	BC20T
RT02	70-08519
RX01/02	BC05L
RX78P	BC80D, BC80E
Tempest	BC20S, BC20U, BC21L
TU10	BC08N, BC08P
TU20	70-05541
TU55	74-05151, BC04X, BC05A
TU56	BC04X, BC04Y, BC05A, BC05B
TU58	BC20Y, BC20Z
TU60	BC05L
TX02	BC10X, BC10Y
TX05	BC10W
UDC	BC40D
VC8E	BC01L, BC01M, 70-08499, 70-08977
VK100	BC26B
VT1XXAH	BC20R
VT05	BC10U, BC99P
VT8E	70-08977, 70-09042